

Trends and Future Challenges of MOSFET, FinFET and GAAFET

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Date of Submission: 15-11-2025

Date of Acceptance: 25-11-2025

ABSTRACT

Semiconductor technologies are advancing at an exceptional pace, evolving from metal–oxide–semiconductor field-effect transistors (MOSFETs) to fin field-effect transistors (FinFETs), and most recently to gate-all-around field-effect transistors (GAAFETs). These device architectures offer substantial potential for the future of electronic components and integrated systems.

This article analyzes the applications, technological challenges, and development prospects of FinFET and GAAFET technologies. Their structural advantages make them highly suitable for low-power systems, high-performance computing, and artificial intelligence applications. However, as transistor dimensions continue to shrink, issues related to heat dissipation, leakage currents, and manufacturing stability become increasingly difficult to control.

Despite these challenges, the future of semiconductor technology remains promising, with multiple pathways for continued innovation—including the adoption of alternative channel materials such as germanium and two-dimensional materials, as well as emerging device architectures such as U-shaped field-effect transistors and complementary field-effect transistors. As the industry continues to pursue smaller and more energy-efficient transistor technologies, breakthroughs in material science and device engineering will play a decisive role in shaping the next generations of semiconductor devices.

Although significant obstacles persist, the semiconductor field continues to evolve rapidly, promising a future in which transistor technologies are more compact, more efficient, and more capable than ever before.

Keywords: Semiconductor technology, MOSFET, FinFET, GAAFET, semiconductor transistors

I. INTRODUCTION

Throughout the history of technology, numerous inventions have marked transformative

milestones in human society. Just as fire, the wheel, and the printing press fundamentally reshaped civilization, semiconductor transistors have become an equally pivotal innovation in the modern era. Although they may not possess the immediate tangibility or dramatic impact of earlier discoveries, the influence of semiconductor transistors on contemporary life is profound and undeniable.

Transistors are not merely semiconductor devices; they form the foundational building blocks of the electronic age. From the earliest bipolar junction transistors to the emergence of metal–oxide–semiconductor field-effect transistors (MOSFETs), followed by the development of fin field-effect transistors (FinFETs), and more recently gate-all-around field-effect transistors (GAAFETs), these devices have driven the exponential advancement of modern electronics.

This article presents a comprehensive overview of transistor evolution, elucidating their operational principles and highlighting how these miniature devices have enabled remarkable technological achievements. We explore the origins of the transistor, the adoption of new materials to enhance device performance, the critical role of semiconductor transistors in device scaling, and the architectural transition from MOSFET to FinFET and ultimately to GAAFET in pursuit of improved efficiency.

For those living in an era of rapid technological progress, understanding semiconductor transistors is not merely an exercise in curiosity—it provides insight into the transformative power of innovation. It reminds us that even the smallest and seemingly simplest technologies can drive sweeping change. Although the future trajectory of transistor development remains uncertain, this article aims to offer a clear perspective on the next potential steps in their ongoing evolution.

II. EVOLUTION OF FIELD-EFFECT TRANSISTORS (FETS)

Over the years, semiconductor transistor technology has undergone significant advancements to meet the increasing demands of the electronics industry. This section presents the evolutionary progression of field-effect transistors, beginning with the traditional MOSFET, followed by the three-dimensional FinFET, and finally the gate-all-around FET (GAAFET), the latest architecture in the scaling roadmap. We examine the operational principles, structural characteristics, and key challenges associated with each technology.

2.1. MOSFET

The metal-oxide-semiconductor field-effect transistor (MOSFET) represents a major milestone in the history of electronic device development. A MOSFET typically consists of a metal gate, an oxide insulating layer, and a semiconductor body. Current flow through the device is modulated by the gate voltage.

The concept of the MOSFET was first proposed in the early twentieth century, and Julius

Edgar Lilienfeld filed the earliest patents for this idea in the 1920s. However, the first functional MOSFET was successfully demonstrated in the 1960s by Dawon Kahng and Martin M. Atalla at Bell Labs [1].

MOSFET operation is based on applying a voltage to the gate, which generates an electric field that modulates the concentration of charge carriers (electrons or holes) within the channel. When the gate voltage attracts carriers into the channel, a conductive path forms and current can flow (the on-state). Conversely, when the gate voltage repels carriers, the channel is depleted and current is suppressed (the off-state). Physically, the MOSFET relies on the junction between p-type and n-type semiconductor regions, where a depletion region is formed. By varying the applied voltage, one can control the conductivity between the source and drain terminals [2].

There are two common MOSFET types, pMOS and nMOS, which differ in the dominant carriers responsible for conduction: holes in pMOS and electrons in nMOS. A comparison of their structures is shown in Figure 1.

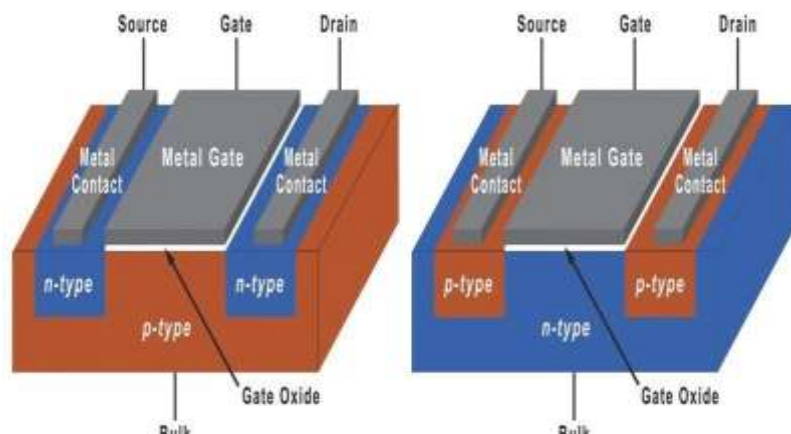


Figure 1: Structural comparison between pMOS and nMOS transistors.

2.2. FinFET

The FinFET-short for fin field-effect transistor-constitutes a major technological advancement beyond traditional MOSFETs. Instead of the planar structure found in MOSFETs, FinFETs employ a three-dimensional silicon “fin” that protrudes above the substrate surface.

This architecture enhances electrostatic control over the channel, mitigates leakage, and significantly improves device performance. A comparison between MOSFET and FinFET structures is presented in Figure 2.

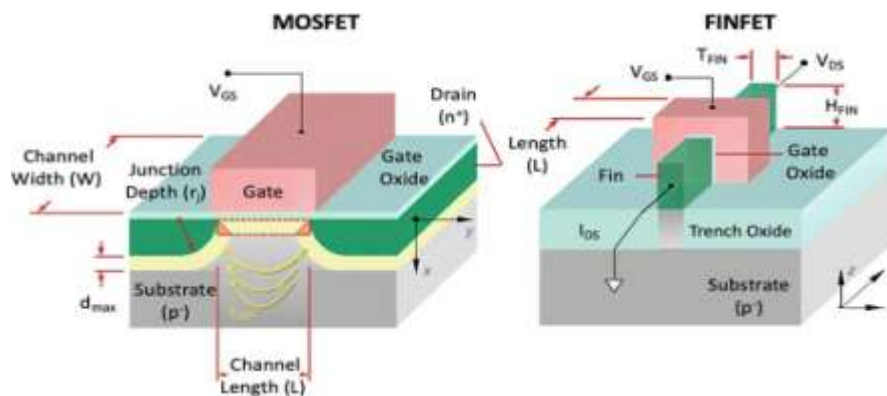


Figure 2: Structural comparison between MOSFET and FinFET.

A notable breakthrough occurred in 1999 when Chenming Hu introduced the FinFET—an innovation that enabled an unprecedented density of transistors on a single chip. The motivation for this development stemmed from the limitations of traditional planar MOSFETs, particularly as transistor dimensions shrank below the micron scale [3].

Fundamentally, MOSFETs and FinFETs operate according to similar electrical principles: current between the source and drain is controlled by the gate voltage. However, their structural differences are substantial. In planar MOSFETs, the gate lies on top of a flat channel, providing limited electrostatic control. In contrast, the FinFET's three-dimensional fin elevates the channel above

the substrate, enabling the gate to wrap around the fin from two or even three sides. This semi-surrounding gate structure offers superior field control and improved suppression of leakage mechanisms.

2.3. GAAFET

Figure 3 illustrates the architectural evolution of field-effect transistors (FETs) across multiple generations. The gate-all-around FET (GAAFET) represents a significant advancement, featuring a gate structure that fully surrounds the channel from all directions. This configuration enables exceptional electrostatic control, reduces leakage, and enhances transistor performance compared with earlier device architectures.

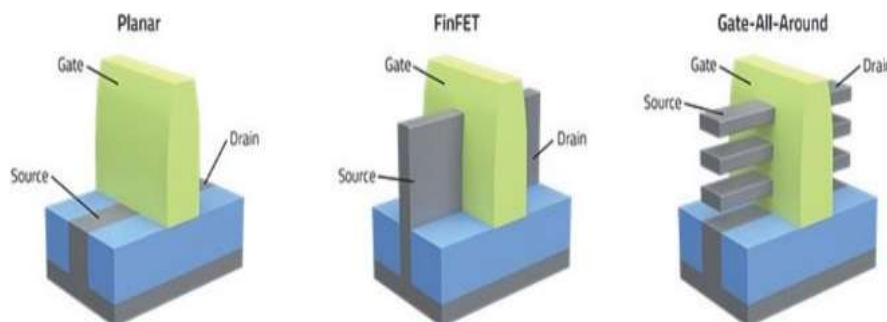


Figure 3: Comparison of MOSFET, FinFET, and GAAFET structures.

Although widely regarded as a next-generation technology today, the concept of the GAAFET dates back to 1988, when a research group at Toshiba—led by Fujio Masuoka, Hiroshi Takato, and Kazumasa Sunouchi—demonstrated a breakthrough vertical nanowire device referred to as the “surrounding-gate transistor” [5].

The fully surrounded gate architecture significantly suppresses short-channel effects (SCE), a dominant issue when transistor dimensions are aggressively scaled. Unlike earlier technologies, where the gate controls the channel

from one or two sides, the GAAFET's all-around gating ensures uniform electrostatic potential distribution, resulting in fast switching characteristics, stable threshold voltages, and substantially reduced leakage currents. Consequently, GAAFETs retain high performance even in low-power or near-off operating conditions [4].

2.4. COMPARISON OF FET STRUCTURES

Traditional planar MOSFETs have been continuously scaled for decades, but they are now

approaching fundamental physical limits associated with short-channel effects and quantum tunneling. These constraints motivated the transition to the three-dimensional FinFET architecture, which offers improved electrostatic control and alleviates several limitations of planar MOSFETs.

However, as dimensions continue to approach the atomic scale, FinFETs themselves encounter new challenges, ultimately leading to the development of GAAFETs. With their fully surrounding gate design, GAAFETs provide superior electrostatic control, marking an important step forward in transistor technology.

As scaling progresses, MOSFETs increasingly suffer from short-channel effects that degrade energy efficiency by increasing leakage currents. FinFETs partially address this issue through their 3D structure, reducing leakage and enhancing performance. Yet, at even smaller dimensions, FinFETs face inherent structural constraints, making GAAFETs the more favorable architecture due to their outstanding electrostatic control capabilities.

With the continuous reduction in transistor dimensions, issues related to threshold voltage (V_{th}) variability and short-channel effects become more severe. In traditional planar MOSFETs, maintaining stable threshold voltage becomes difficult as SCE leads to threshold roll-off, increased leakage, and drain-induced barrier lowering (DIBL). FinFETs improve gate control to some extent, thereby mitigating these problems, but still cannot fully eliminate them as scaling continues.

By contrast, GAAFETs—with their nearly ideal gate-all-around geometry—offer far superior SCE suppression. The uniform potential distribution within the channel effectively minimizes short-channel behavior and ensures stable, energy-efficient operation at advanced technology nodes.

III. APPLICATIONS OF FIELD-EFFECT TRANSISTORS (FETS)

The advancement of field-effect transistor (FET) technologies has enabled a wide range of transformative applications, revolutionizing multiple industries and driving technological progress across diverse domains. As transistor architectures have evolved, their integration into electronic systems has become increasingly specialized, with each generation of FETs providing advantages tailored to specific requirements. This section highlights prominent

applications of MOSFET, FinFET, and GAAFET technologies in various fields.

3.1. MOSFET

In power electronics and control systems, MOSFETs play a critical role in switching and regulating electrical currents. At high operating frequencies, MOSFETs significantly reduce switching losses—one of the primary contributors to energy dissipation in electronic devices. Consequently, MOSFET driver circuits are designed to rapidly activate and deactivate these semiconductor switches. Power MOSFETs, specifically engineered for high-current operation, are widely used in switch-mode power supplies and motor control units [6].

In digital logic and computing, MOSFETs function as electronic switches that regulate current flow, forming the fundamental building blocks of digital logic circuits. Modern central processing units (CPUs) and graphics processing units (GPUs) integrate millions or even billions of MOSFETs. Continued MOSFET scaling down to the nanometer regime has sustained Moore's law and enabled progressive increases in transistor density [7].

In memory technologies, conventional static random-access memory (SRAM) utilizes MOSFET-based flip-flop structures to store data, whereas dynamic random-access memory (DRAM) stores charge within a MOS capacitor—a derivative of the MOSFET structure. Modern non-volatile memory technologies such as EEPROM, EPROM, and flash memory also rely on floating-gate MOSFETs as their fundamental storage elements [8].

Finally, MOSFET technologies play an essential role in sensing and imaging. CMOS and CCD image sensors use MOSFETs for photodetection and signal processing. Moreover, MOS-based structures have been widely employed in chemical and biological sensors due to their sensitivity and compatibility with integrated circuit fabrication [9].

3.2. FinFET

The introduction of FinFET technology has brought substantial improvements to electronic applications, particularly in low-power digital logic systems. Recent studies have shown that negative-capacitance FinFETs (NC-FinFETs) can significantly reduce delay and power consumption compared with conventional FinFETs. These characteristics make NC-FinFETs highly suitable

for energy-efficient applications such as embedded inverters, ring oscillators, and two-bit full adders.

In the domains of memory and artificial intelligence (AI), compute-in-memory (CIM) architectures utilizing 6T-SRAM cells based on FinFET technology have been developed to mitigate data-movement bottlenecks in deep neural networks. The transition to three-dimensional FinFET structures enhances design density, reduces power consumption, and improves overall performance.

In computational applications, the design of FinFET-based 1-bit full adders is crucial for digital systems such as microprocessors and digital signal processors. Research indicates that FinFET technology enables more energy-efficient, lower-latency, and smaller-area 1-bit adder circuits, contributing to improved performance in complex digital architectures.

3.3. GAAFET

GAAFET technology, distinguished by its superior electrostatic control, is rapidly gaining adoption across multiple high-performance and low-power application domains. One of its most significant applications lies in high-performance computing (HPC) and server-class processors. Due to their improved energy efficiency and enhanced performance characteristics, GAAFET-based CPUs can operate at higher clock frequencies while maintaining lower power consumption—an essential requirement for data centers and large-scale server infrastructures.

In low-power electronics, the energy efficiency of GAAFETs, combined with their capability to operate at ultra-low supply voltages, makes them ideal for wearable devices and Internet of Things (IoT) systems, enabling longer battery life without compromising performance.

In emerging memory technologies, devices such as magnetic random-access memory (MRAM) and resistive random-access memory (ReRAM) can benefit substantially from the reduced leakage and enhanced energy efficiency offered by GAAFETs. Several studies have shown that GAAFET-based SRAM cells exhibit superior stability and performance, making them suitable for low-power memory applications [11].

In artificial intelligence, the rapid expansion of deep learning models requires hardware capable of intensive computation. With their fast switching speeds and improved current control, GAAFET devices are increasingly used in specialized AI accelerators for neural networks and machine learning workloads, significantly

enhancing computation efficiency for complex AI algorithms.

Finally, in the telecommunications sector—particularly with the emergence of 5G-GAAFETs—are considered highly promising. High-frequency data transmission requires transistors capable of operating at elevated frequencies while maintaining low power consumption. Several GAAFET structures have been proposed to suppress drain-induced barrier lowering (DIBL) and optimize performance for radio-frequency (RF) applications. These attributes suggest that GAAFETs could play a key role in next-generation RF transceivers and 5G modem designs.

IV. FUTURE TRENDS IN FIELD-EFFECT TRANSISTOR (FET) DEVELOPMENT

The semiconductor industry continues to advance rapidly, yet these advancements are accompanied by increasingly complex challenges. As technology progresses beyond conventional limits and adopts novel device architectures, semiconductor transistors face substantial technical and physical constraints. At the same time, the dynamic nature of the industry creates new opportunities for innovation, enabling breakthroughs that may fundamentally reshape modern electronics. This section highlights the current challenges and the emerging future directions in transistor development.

4.1. CHALLENGES IN THE EVOLUTION OF SEMICONDUCTOR TRANSISTORS

The transition from MOSFET to FinFET and now to GAAFET promises a bright future for electronic technologies. However, this evolutionary pathway also presents numerous difficulties.

As transistor dimensions shrink toward the atomic scale, current lithography and fabrication methods approach their fundamental limits. Achieving the required precision at such small dimensions is increasingly difficult. Furthermore, the compact device geometries complicate heat dissipation, since high operating temperatures can degrade performance and reduce device reliability.

Another major challenge involves leakage currents and performance variability. Despite technological improvements, quantum mechanical phenomena—such as tunneling and increased leakage—become more pronounced at extremely small dimensions. Variations in fabrication processes can also lead to device-to-device inconsistencies, resulting in unpredictable transistor behavior.

From a materials perspective, the introduction and integration of new materials into advanced transistor nodes require novel approaches to ensure compatibility with existing manufacturing processes.

As scaling continues, transistors become more susceptible to degradation mechanisms such as hot-carrier injection, thermal instability, and long-term dielectric breakdown.

Moreover, quantum effects such as tunneling make transistor behavior increasingly difficult to predict. Undesired currents may appear even when the device is nominally off, complicating efforts to maintain energy efficiency and device reliability.

4.2. PROSPECTS FOR TRANSISTOR TECHNOLOGIES BEYOND GAAFET

Although significant advancements have been made from MOSFET to GAAFET, the semiconductor industry continues to seek even smaller and more efficient transistor architectures. Emerging innovations are now pointing toward a future that extends beyond the GAAFET paradigm.

One promising direction is the development of alternative channel materials to replace traditional silicon. For example, germanium is regarded as a promising candidate due to its potential to improve electrostatic characteristics. In addition, two-dimensional (2D) materials—such as graphene and transition metal dichalcogenides (TMDCs)—are expected to offer advantages including high carrier mobility and enhanced channel controllability.

Beyond materials, architectural design innovations play a crucial role in sustaining device performance as scaling progresses. For instance, the U-shaped field-effect transistor (UFET) has emerged with a more compact gate structure and reduced leakage, making it a potential candidate to replace existing device geometries.

Furthermore, hybrid designs such as the complementary field-effect transistor (CFET) are gaining attention. CFET technology vertically stacks nMOS and pMOS devices, eliminating the traditional lateral separation between them. This vertical integration enhances channel efficiency and improves current control. Such architectural innovations may represent a significant step forward in the future evolution of semiconductor transistor technologies

V. CONCLUSION

The rapid advancement of semiconductor transistor technologies—from MOSFET to FinFET

and GAAFET—has paved the way for a highly promising future in electronic devices and integrated systems. However, alongside these achievements, several critical challenges remain to be addressed, including dimensional scaling limits, thermal management issues, leakage currents, and manufacturing stability.

In addition, integrating new transistor architectures into existing systems and adopting novel materials introduces compatibility and reliability concerns. Despite these obstacles, the overall outlook for semiconductor transistor technology remains optimistic.

Research on alternative channel materials, such as germanium and two-dimensional materials, is expected to play a pivotal role in the next stages of development. At the same time, emerging architectural innovations—such as U-shaped FETs and complementary FETs (CFETs)—offer the potential to succeed traditional GAAFET structures as future transistor generations.

Although numerous challenges persist, the field of semiconductor transistor technology continues to be defined by relentless innovation. We can anticipate the emergence of next-generation transistor architectures that are more efficient, more compact, and more capable in the near future.

REFERENCES

- [1]. Charboneau, T. *The Fathers of the MOSFET: Dawon Kahng and Martin Atalla*. All About Circuits, 2021.
- [2]. Teja, R. *Introduction to MOSFET | Enhancement, Depletion, Amplifier, Applications*. Electronics Hub, 2021.
- [3]. Chung, H. T., Shih, B. J., Duong, C. C., et al. "Single-Crystalline Ge Islands (Ge-SCI) Engineering and BEOL Ge FinFET Switch Arrays on Top of Si Circuits for Monolithic 3D Regulators." *IEDM 2021 – IEEE International Electron Devices Meeting, IEEE, 2021*, pp. 34.5.1–34.5.4.
- [4]. Erin, Z. *Semiconductor Engineering: Gate-All-Around FET (GAAFET) – A Viable Alternative to FinFET Design*. 2023.
- [5]. Li, Y., Kanazawa, K., Izawa, T., et al. "1.5-nm Node Surrounding-Gate Transistor (SGT) SRAM Cell with Staggered Pillars and a Self-Aligned Process for Gate, Bottom Contacts, and Pillars." *IEEE International Memory Workshop (IMW), 2021*, pp. 1–4.

- [6]. Duong, C. N. MOSFET/IGBT Driver Theory and Applications. Application Note AN002, 2001.
- [7]. Ong, W. Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET). Target Technology, 2023.
- [8]. Jaisawal, R. K., Kondekar, P. N., Yadav, S., et al. “Insights into Negative-Capacitance FinFET Operation for Low-Power Logic Applications.” *Microelectronics Journal*, 2022, 119: 105321.
- [9]. Gul, W., Shams, M., Al-Khalili, D. “FinFET 6T-SRAM All-Digital Compute-in-Memory for Artificial Intelligence Applications: A Review and Analysis.” *Computers*, 2023, 14(8): 1535.
- [10]. Pittala, C., Vijay, V. “Design of FinFET 1-Bit Full Adder Circuits for Computational Applications.” *International Conference on Emerging Applications of Information Technology*. Singapore: Springer, 2021, pp. 590–596.
- [11]. Kumar, A., Pattanaik, M., Srivastava, P., et al. “GAAFET-Based SRAM Cell for Enhanced Stability in Low-Power Applications.” *Silicon*, 2022, 14(13): 8161–8172.
- [12]. Kumar, A., Pattanaik, M., Srivastava, P., et al. “Mitigation of Drain-Induced Barrier Lowering in DM-HD-No GAAFET for Radio-Frequency Applications.” *IET Circuits, Devices & Systems*, 2020, 14(3): 270–275.
- [13]. Day, Y. K., Bhattacharyya, T. K. “Opportunities in Device Scaling at the 3-nm Node and Beyond: FinFET vs. GAAFET vs. UFET.” *IEEE Transactions on Electron Devices*, 2020, 67(6): 2633–2638.
- [14]. Imec. Imec Places Complementary FET (CFET) on the Technology Roadmap. *Imec-int*, 2023.