

# On the Optimal Strategy for Circuit Design

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**ABSTRACT:** The circuit optimization process is defined as a controlled dynamic system with a special control vector. This vector serves as the main tool for generalizing the problem of circuit optimization and produces a huge number of different optimization strategies. In this case, we can formulate the task of finding the best optimization strategy that minimizes processor time. We need to find the optimal structure of the control vector that minimizes processor time. A special function, which is a combination of the Lyapunov function of the optimization process and its time derivative, was proposed to predict the optimal structure of the control vector. The found optimal positions of the switching points of the control vector give a large gain in CPU time in comparison with the traditional approach.

**KEYWORDS:** Circuit optimization, Control theory approach, Controllable dynamic system, Lyapunov function.

## I. INTRODUCTION

Reducing computational time when designing large systems is one of the sources of overall improvement in design quality. This problem is of great importance because it has many applications, for example, for designing electronic circuits of VLSI. Any traditional system design strategy includes two main parts: the analysis of mathematical model of the physical system and optimization procedure that achieves the optimum point of cost function of designing.

There are several powerful methods that reduce the time required to analyze the circuit. Since the matrix of the large-scale scheme is very sparse, special methods of the sparse matrix are successfully used for this purpose [1]. Other approach to reducing the amount of computation is based on decomposition methods. An extension of direct solution methods can be obtained by hierarchical decomposition and macro model presentation [2]. Another approach to achieving decomposition at a nonlinear level is to use special

iteration methods and implemented in [3] for the iterated timing analysis and circuit simulation.

The methods for optimizing analog circuits can be divided into two main groups: deterministic optimization methods and stochastic search algorithms. Some of the drawbacks of classical deterministic optimization algorithms are the requirement of a good starting point in the parameter space, the unsatisfactory local minimum that can be achieved, and very often the requirement of continuity and differentiability of the goal function. To overcome these problems, some special methods were applied. For example, geometric programming methods [4], guarantee convergence to a global minimum, but, on the other hand, this requires a special formulation of equations and poses additional difficulties.

In recent years, stochastic search algorithms have been developed, especially evolutionary computation algorithms such as genetic algorithms (GA), differential estimates, genetic programming, etc. [5]-[7]. GA was used as optimization routine for analog circuits because of its ability to find a satisfactory solution. A special algorithm defined as a particle swarm optimization (PSO) technique is one of the evolutionary algorithms and competes with GA [8]-[10]. In recent years, articles have appeared using the neural networks approach to optimize analogue circuits [11]-[13]. However, in this case, apparently, one does not need to rely on a significant reduction in optimization time.

The practical aspects of deterministic methods were developed for the design of electronic circuits with various optimization criteria [14]. The fundamental problems of developing the structure and adaptation of automation design systems were considered in some works [15], [16].

The ideas of designing the system described above as deterministic and stochastic can be called the traditional approach or the traditional strategy, since the analysis method is based on the laws of Kirchhoff.

The idea of rejecting Kirchhoff's laws when designing electronic circuits was implemented in two design systems [17], [18]. The most general approach was implemented in the development of a generalized methodology for the process of optimization of an electronic circuit, defined as a controlled dynamic system [19]. With this approach, a traditional design strategy is just one representative of a wide range of different design strategies. The potential gain in computer time that can be obtained by this approach increases when the size and complexity of the system increases.

## II. PROBLEM FORMULATION

The design process of any analog system can be defined in discrete form [19] as the task of minimizing the generalized cost function  $F(X, U)$  using system (1) with constraints (2):

$$X^{s+1} = X^s + t_s H^s, \quad (1)$$

$$(1 - u_j)g_j(X) = 0, \quad j = 1, 2, \dots, M, \quad (2)$$

where  $X = (X', X'')$ ,  $X' \in \mathbb{R}^K$ , is a vector of independent variables,  $X'' \in \mathbb{R}^M$  is a vector of dependent variables,  $M$  is the number of the circuit's dependent variables,  $K$  is the number of independent variables,  $N$  is the total number of variables ( $N = K + M$ ) and  $t_s$  is an iteration parameter,  $t_s \in \mathbb{R}^1$ . Additional restrictions, as the positive definiteness of some independent variables, are easily included in the general optimization procedure, as shown by specific examples. Equation (1) describes a minimization procedure, and the function  $H \equiv H(X, U)$  determines the direction in which the generalized goal function  $F(X, U)$  decreases. The functions  $g_j(X)$  for all  $j$  define the equations of the circuit model. The components of control vector  $U$  are a set of control functions:  $U = (u_1, u_2, \dots, u_M)$ , where  $u_j \in \Omega$ ,  $\Omega = \{0; 1\}$ . The complete set of different optimization strategies includes  $2^M$  strategies. This set can be called a structural basis. The generalized goal function  $F(X, U)$  can be defined, as follows:

$$F(X, U) = C(X) + \varphi(X, U) \quad (3)$$

where  $C(X)$  is a non-negative goal function of the design process, and  $\varphi(X, U)$  is an additional penalty function:

$$\varphi(X, U) = \frac{1}{\varepsilon} \sum_{j=1}^M u_j \cdot g_j^2(X), \quad (4)$$

where  $\varepsilon$  is an additional coefficient used to adapt the penalty function.

This formulation of the problem permits to redistribute the computational time between the problems (1) and (2). The control vector  $U$  is the main tool of this methodology. The task of finding the optimal design strategy is formulated in this case as a typical task to minimize the functional of control theory. The functional that needs to be minimized is the total CPU time  $T$  of the design process. This functional directly depends on the number of operations and on the design strategy that has been implemented. We need to know the optimal dependencies of all control functions  $u_j$ .

A continuous form of task definition is more adequate for applying control theory. This continuous form replaces Eq. (1) and can be represented as follows:

$$\frac{dx_i}{dt} = f_i(X, U), \quad i = 1, 2, \dots, N, \quad (5)$$

This system, together with equations (2), (3) and (4), constitutes a continuous form of the design process. The structural basis of a set of strategies corresponding to a fixed control vector includes  $2^M$  different strategies. The functions of the right-hand side of system (5) are defined, for example, for the gradient method, as:

$$f_i(X, U) = -\frac{\delta}{\delta x_i} F(X, U), \quad i = 1, 2, \dots, K, \quad (6)$$

$$f_i(X, U) = -u_{i-K} \frac{\delta}{\delta x_i} F(X, U), \\ + \frac{(1 - u_{i-K})}{dt} \left\{ -x_i^s + \mu_i(X) \right\} \\ i = K+1, K+2, \dots, N, \quad (6')$$

where the operator  $\delta / \delta x_i$  hear and below means

$$\frac{\delta}{\delta x_i} \rho(X) = \frac{\partial \rho(X)}{\partial x_i} + \sum_{p=K+1}^{K+M} \frac{\partial \rho(X)}{\partial x_p} \frac{\partial x_p}{\partial x_i}, \text{ and}$$

determines the application of the gradient method for a complex function that has both independent and dependent variables,  $x_i^s$  equals  $x_i(t - dt)$ ; and  $\mu_i(X)$  is the implicit function ( $x_i = \mu_i(X)$ ) determined by the system (2).

Control functions  $u_j$  are time-dependent in the general case. In this context, the goal of optimal control is to minimize the cost function  $F(X, U)$  for the shortest possible CPU time. The functions  $f_i(X, U)$  are piecewise continuous and their structure can be found by approximate methods of control theory [20].

### III. LYAPUNOV FUNCTION

Based on the analysis presented in the previous section, we can conclude that the time-optimal algorithm can be constructed as a set of different strategies with several switching points from one strategy to another.

From the set of optimization strategies that exist within the framework of the structural basis, two specific strategies can be distinguished, the traditional optimization strategy (TOS), when  $u_j=0$  for all  $j$  and the modified traditional optimization strategy (MTOS), when  $u_j=1$  for all  $j$ . As shown in [21] it is necessary to switch the control vector from MTOS to TOS in order to obtain a special super-acceleration effect. The main problem of constructing a time-optimal algorithm is the unknown optimal sequence of switching points in the design process. We need to define a special criterion that allows us to implement an optimal or quasi-optimal algorithm by searching for optimal switching points. It is known that the Lyapunov function of a dynamic system serves as a very informative object for analyzing the behavior of a system in the framework of control theory. We suggest using the Lyapunov function of the design process to determine the main characteristics of the optimal algorithm, in particular, to search for optimal switching points.

There is freedom of choice of the Lyapunov function due to the non-unique form of this function. Let us define the Lyapunov function of the design process (2)-(6) by the following expression:

$$V(X, U) = [F(X, U)]^T \quad (7)$$

The function (7) satisfies all the conditions of the standard definition of the Lyapunov function.

We can define the design process as a transient process of a controlled dynamic system that can provide a stationary point (the end point of the optimization procedure) for some time. The task of constructing an algorithm of time-optimal design can now be formulated as the task of finding a transient process with a minimum transition time. The idea of minimizing the transition process time by means of a special choice of the right-hand side of the main system of equations is well known [22]; in our case, these are the functions  $f_i(X, U)$ . It is necessary to change the functions  $f_i(X, U)$  by choosing the control vector  $U$  to obtain the maximum rate of decrease of the Lyapunov function (the maximum absolute value of the time derivative

of the Lyapunov function  $\dot{V} = dV/dt$ ). Now we can define a more informative function as the time

derivative of the Lyapunov function relative to the

Lyapunov function:  $W = \dot{V}/V$ . In this case, we can compare various design strategies using the behavior of the function  $W(t)$  to find the optimal position for the switching points of the control vector.

### IV. RESULTS AND DISCUSSION

All examples were analyzed for the continuous form of the optimization procedure (5). The functions  $V(t)$  and  $W(t)$  were the main objects of analysis, and their behavior was analysed during the design process. It is interesting to analyze the behavior of the function  $V(t)$  to determine the optimal position of the switching points of the control vector. This function serves as a sensitive criterion for determining the optimal switching of the control vector  $U$ . The Lyapunov function  $V(t)$  for all examples was calculated by formula (8) with  $r=0.5$ .

#### 4.1 Example 1

An analysis of the design process of the three-node passive nonlinear circuit shown in Figure 1 is presented below.

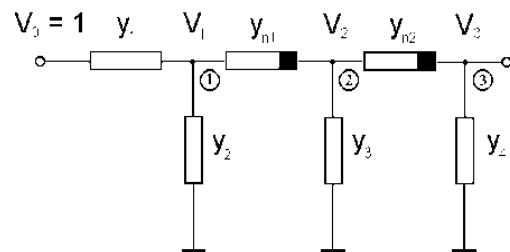


Figure 1: Three-node nonlinear passive circuit

The nonlinear elements are defined as:

$y_{nl} = a_{nl} + b_{nl} \cdot (V_1 - V_2)^2$ ,  $y_{n2} = a_{n2} + b_{n2} \cdot (V_2 - V_3)^2$ . The vector  $X$  includes seven components:  $x_1^2 = y_1$ ,  $x_2^2 = y_2$ ,  $x_3^2 = y_3$ ,  $x_4^2 = y_4$ ,  $x_5 = V_1$ ,  $x_6 = V_2$ ,  $x_7 = V_3$ . The meaning of introducing squares for variables  $x_i$  corresponds to overcoming additional restrictions on the positive definiteness of conductivities  $y_i$ .

The mathematic model (2) of this network includes three equations ( $M=3$ ):

$$g_1(X) \equiv -x_1^2 + (x_1^2 + x_2^2)x_5 + [a_{nl} + b_{nl}(x_5 - x_6)](x_5 - x_6) = 0$$

$$g_2(X) \equiv x_3^2 x_6 + [a_{n1} + b_{n1}(x_5 - x_6)^2](x_6 - x_5) \quad (8)$$

$$+ [a_{n2} + b_{n2}(x_6 - x_7)^2](x_6 - x_7) = 0$$

$$g_3(X) \equiv x_4^2 x_7 + [a_{n2} + b_{n2}(x_6 - x_7)^2](x_7 - x_6) = 0$$

The optimization procedure (5) includes seven equations. This network is characterized by three dependent parameters and the control vector includes three control functions:  $U = (u_1, u_2, u_3)$ .

The goal function  $C(X)$  is defined by the formula:

$$C(X) = (V_1 - V_2 - k_1)^2 + (V_2 - V_3 - k_2)^2 + (V_3 - k_3)^2.$$

The structural basis of strategies includes eight different strategies with the corresponding control vector: (000), (001), (010), (011), (100), (101), (110), and (111). The CPU time for TOS is 1.34 sec. The behavior of the functions  $V(t)$  and  $W(t)$  helps us determine the optimal position of the switching point of the control vector.

Taking into account preliminary considerations about the optimal structure of the algorithm, we analyzed a two-part strategy. The first part is determined by the control vector (111), which corresponds to MTOS, and the second part is determined by the control vector (000), which corresponds to TOS. Thus, switching is carried out between these two strategies.

The optimal position of the switching point was the main goal of this analysis. A sequential change of the switching point was implemented for the integration step number from 2 to 20.

The behavior of the functions  $V(t)$  and  $W(t)$  during the design process after the switching point is shown in Figure 2.

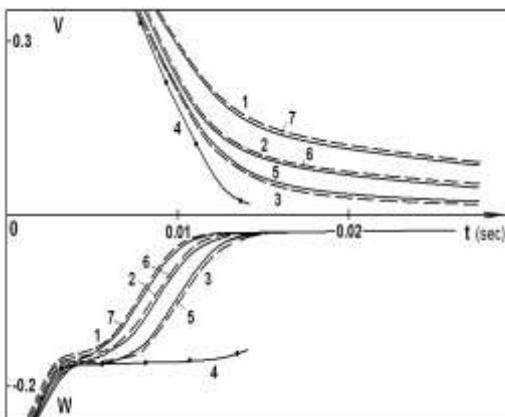


Figure 2: Behavior of the functions  $V(t)$  and  $W(t)$  during the design process for seven different switch points (from 6 to 12)

As discussed above, the main element of the fast algorithm is the optimal position of the switching point of the control vector. Figure 2 shows the behavior of the functions  $V(t)$  and  $W(t)$  for seven different positions of the switching point. The corresponding total number of iterations and computer time are presented in Table 1.

Table 1: Iterations number and computer time for strategies with different switch points for circuit in Figure 1

N	Switch point	Iterations number	Total design time (sec)
1	6	8409	0.659
2	7	6408	0.502
3	8	3141	0.246
4	9	180	0.014
5	10	3310	0.259
6	11	5918	0.464
7	12	7404	0.581

Integration of system (5) was carried out with a constant step. The analysis shows that the optimal switching point corresponds to step 9 (graph 4 with dots in Figure 2). The analysis shows that the optimal switching point corresponds to step 9 (graph 4 with dots in Figure 2). Curves 1, 2, and 3 correspond to the position of the switching point before the optimal point (curve 4), but curves 5, 6, and 7 correspond to the switching point that is after the optimal one. There is a decrease in computer time from curve 1 to curve 4. On the contrary, computer time increases from curve 4 to curve 7. It means that curve 4 corresponds to the optimal position of the switching point.

The initial part of the dependence of the function  $W(t)$  in Figure 2 is shown in Figure 3 on a large scale.

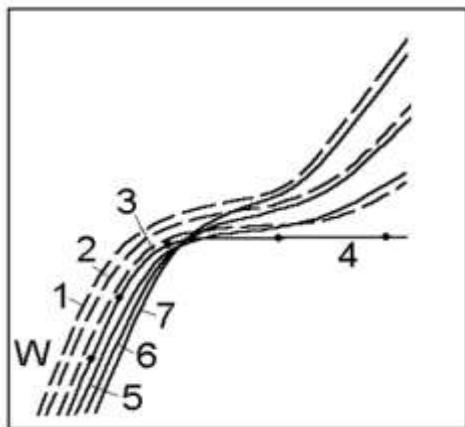


Figure 3: Behavior of the functions  $V(t)$  and  $W(t)$  during the initial part of design process

It can be seen that curves 1, 2, and 3, which correspond to switching points in front of the optimal point (4), have no intersections. On the other hand, curves 5, 6, and 7, obtained for the switching point after the optimal one, have intersections, and each curve lies above curve 4, starting from a certain step. This means that from this moment the graph  $W(t)$  for the optimal switching point lies below all other graphs. Thus, on the one hand, the optimal switching point corresponds to the minimum computer time, on the other hand, this point corresponds to the graph of the function  $W(t)$ , which lies below all other graphs. This property again serves as the main criterion for choosing the optimal switching point. The function  $W(t)$ , which corresponds to the optimal switching point, has a maximum absolute value, starting from the 15th step of integration. This means that at this stage of integration, we can confidently predict the optimal position of the switching point, which will lead to minimal computing time. The optimal strategy is 95 times faster than TOS.

#### 4.2 Example 2

The following example corresponds to a single-stage transistor amplifier in Figure 4.

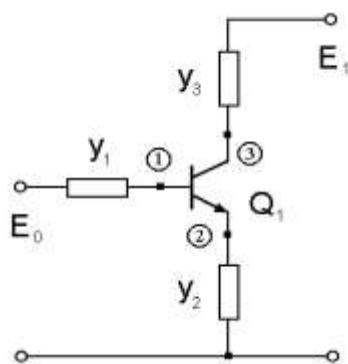


Figure 4: One-stage transistor amplifier

Vector  $X$  includes six components:  $x_1^2 = y_1$ ,  $x_2^2 = y_2$ ,  $x_3^2 = y_3$ ,  $x_4 = V_1$ ,  $x_5 = V_2$ ,  $x_6 = V_3$ . The model of this circuit (2) includes three equations ( $M=3$ ) and the optimization procedure (5) includes six equations. The structural basis contains eight different design strategies. The control vector includes five control functions:  $U = (u_1, u_2, u_3)$ . A static Ebers-Mall model of transistor was used [23]. The goal function  $C(X)$  is determined by the formula  $C(X) = [(x_5 - x_4) - m_1]^2 + [(x_6 - x_4) - m_2]^2$ , where  $m_1, m_2$  are the required voltage values at the transistor junctions. The CPU time for TOS is 26.97 sec.

Figure 5 shows the behavior of the functions  $V(t)$  and  $W(t)$  in the design process with different switching points.

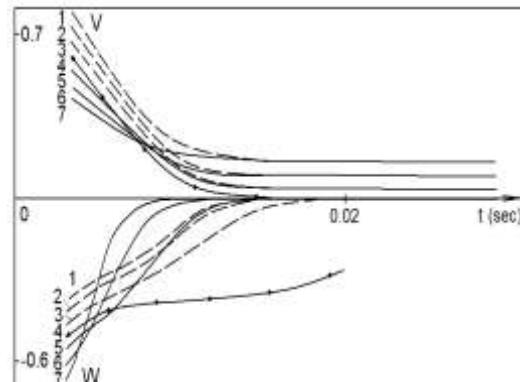


Figure 5: Behavior of the functions  $V(t)$  and  $W(t)$  during the design process for seven different switch points (from 33 to 39) for circuit in Figure 4

The behavior of these functions helps us determine the optimal position of the switching point of the control vector. We analyzed the strategy, which consists of two parts. The first part is determined by the control vector (111), which corresponds to MTOS, and the second part is determined by the control vector (000), which corresponds to TOS. The optimal switching point was the goal of the analysis. A sequential change of the switching point was implemented for integration steps from 2 to 50. The behavior of the functions  $V(t)$  and  $W(t)$  for the switch points from 33 to 39 are shown in this figure and the data, which correspond to these graphs, are presented in Table 2.

Table 2: Iterations number and computer time for strategies with different switch points for single-stage transistor amplifier in Figure 4

N	Switch point	Iterations number	Total design time (sec)
1	33	2433	0.404
2	34	2180	0.361
3	35	1748	0.289
4	36	121	0.02
5	37	1705	0.281
6	38	2111	0.349
7	39	2349	0.389

The analysis shows that the optimal switching point corresponds to step 36 (a graph with dots). Computer time has a minimum value for this step. We see that the function  $W(t)$  has a maximum absolute value for the optimal switching step (number 4), starting from the 55th integration step. We observe the specific behavior of the function  $W(t)$  near the optimal position of the switching point. Before the optimal switching point, the graphs of the function  $W(t)$  are “parallel”. The function  $W(t)$  has a maximum negative value for optimal switching points. The graphs of the function  $W(t)$  that correspond to the optimal position of the switching point (number 4) and before the optimal position (1, 2 and 3) do not intersect. After the optimal points, the graphs of the function  $W(t)$  intersect the graphs that correspond to the optimal switching point and before the optimal one. This means that we can confidently predict the optimal position of the switching points in the initial part of the design process. Optimal strategy is faster than TOS 1348 times.

#### 4.3 Example 3

The last example corresponds to the optimization process for the amplifier with feedback shown in Figure 6.

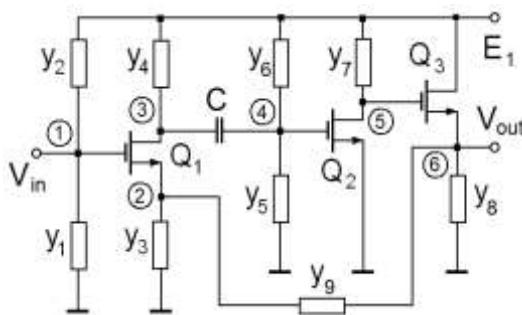


Figure 6: Amplifier with feedback

In this case, we can define nine independent variables  $y_1, y_2, y_3, y_4, y_5, y_6, y_7, y_8, y_9$

( $K=9$ ) and six dependent variables  $V_1, V_2, V_3, V_4, V_5, V_6$ , ( $M=6$ ) for TOS. The vector  $X$  includes 15 components:  $x_1^2 = y_1, x_2^2 = y_2, \dots, x_9^2 = y_9, x_{10} = V_1, x_{11} = V_2, \dots, x_{15} = V_6$ . The model of this circuit (2) includes six equations ( $M=6$ ) and the optimization procedure (5) includes 15 equations. The structural basis contains 64 different design strategies. The control vector includes six control functions:  $U = (u_1, u_2, \dots, u_6)$ . The goal function  $C(X)$  is determined by the formula

$$C(X) = (x_{10} - x_{11} - m_1)^2 + (x_{12} - x_{11} - m_2)^2 + (x_{13} - m_3)^2 + (x_{14} - m_4)^2 + (x_{15} - m_5)^2 + (E_1 - x_{15} - m_6)^2$$

where  $m_1, m_2, m_3, m_4, m_5, m_6$  are the before-defined values of voltages on GS and DS for  $Q_1, Q_2$  and  $Q_3$ . These parameters were defined as:  $m_1=-1.8$  V,  $m_2=6.8$  V,  $m_3=-2.0$  V,  $m_4=6.8$  V,  $m_5=-1.5$  V,  $m_6=6.0$  V. The CPU time for TOS is 1426.7 sec.

A quasi-optimal strategy can be composed as a combination of MTOS and TOS with two switching points. The first switching point corresponds to the  $n$ -th step of optimization procedure and changing the control vector from (1111111111) to (0000000000), and the second switching point corresponds to the  $n+6$ -th step and changing the control vector from (0000000000) to (1111111111).

The optimal distribution of switching points over the behavior of the Lyapunov function  $V(t)$  and its time derivative  $W(t)$  is analysed.

The behavior of the functions  $V(t)$  and  $W(t)$  is shown in Figure 7 for various switching points. All graphs start from the point that lies at the 40th step of the optimization procedure.

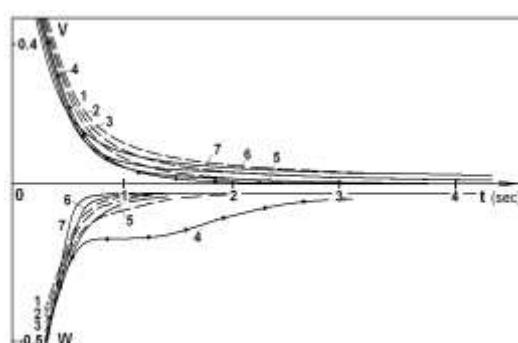


Figure 7: Behavior of the functions  $V(t)$  and  $W(t)$  during the design process for seven different switch points (from 10 to 16) for circuit in Figure 6

The total number of iterations and computing time are presented in Table 3 for some switching points close to optimal.

Table 3: Iterations number and computer time for strategies with different switch points for amplifier in Figure 6

N	Switch point 1	Switch point 2	Iterations number	Total design time (sec)
1	10	16	8187	154.31
2	11	17	7432	140.04
3	12	18	4797	90.36
4	13	19	167	3.14
5	14	20	8405	158.41
6	15	21	11610	218.81
7	16	22	12372	233.16

Integration of system (1) was carried out using an optimal integration step. As in the previous example, the optimization algorithm was proposed as a combination of MTOS and TOS. In this case, the quasi-optimal control vector includes two switching points. We change the control vector from (11111111111) to (00000000000) and from (00000000000) to (11111111111). A sequential change of the switching point was implemented for the integration step number from 2 to 25. The behavior of the functions  $V(t)$  and  $W(t)$  for the optimal switching step and some steps near the optimal one confidently determines the optimal position of the switching point. The function  $W(t)$  has a maximum negative value for the optimal switching point. The graphs of the function  $W(t)$  that correspond to the optimal position of the switching point (number 4) and before the optimal position (1, 2 and 3) do not intersect. After the optimal point, the graphs of the function  $W(t)$  intersect with the graphs that correspond to the optimal switching point. This means that we can determine the optimal position of the switching points during the initial interval of the design process. Optimal strategy is faster than TOS 454 times.

## V. CONCLUSION

We observe a specific behavior of the function  $W(t)$  near the optimal switch point's position. Before the optimal switch point the function  $W(t)$  graphs are "parallel". Function  $W(t)$  has the maximum negative value for the optimal switch points. The graphs of the function  $W(t)$  that correspond to the optimal switch point's position and before the optimal position have not intersection. After the optimal points the graphs of the function  $W(t)$  intersect the graphs that

correspond to the optimal switch point and before the optimal one. It means that we can detect the optimal position of the switch points during the initial design interval.

So, the structure of the optimal control vector i.e. the structure of the time optimal design strategy can be defined by means of the analysis of the relative time derivative of the Lyapunov function during the initial time interval of the design process. The Lyapunov function of the design process contains sufficient information to select the optimal control vector that gives the minimum CPU time.

## REFERENCES

- [1]. Osterby, O.; and Zlatev, Z., 1983, Direct Methods for Sparse Matrices, Springer-Verlag, New York.
- [2]. Rabat, N.; Ruehli, A.E.; Mahoney, G.W.; and Coleman, J.J., 1985, "A Survey of Macromodeling", IEEE Int. Symposium Circuits Systems, pp. 139-143.
- [3]. George A., 1984, "On Block Elimination for Sparse Linear Systems", SIAM J. Numer. Anal., 11, no. 3, pp. 585-603.
- [4]. Hershenson, M.; Boyd, S.; and Lee, T., 2001, "Optimal design of a CMOS op-amp via geometric programming", IEEE Transactions on Computer-Aided Design of Integrated Circuits, 20, no.1, pp.1-21.
- [5]. Srivastava, A.; Kachru, T.; and Sylvester, D., 2007, "Low-power-design space exploration considering process variation using robust optimization", IEEE Trans CAD of Integrated Circuits, 26, no. 1, pp. 67-79.
- [6]. Liu, B.; Wang, Y.; Yu, Z.; Liu, L.; Li, M.; Wang, Z.; Lu, J.; and Fernandez, F.V., 2009, "Analog circuit optimization system based on hybrid evolutionary algorithms", Integration the VLSI journal, 42, no. 2, pp. 137-148.
- [7]. Carneiro, M.L.; de Carvalho, P.H.P.; Deltimple, N.; da C Brito, L.; de Menezes, L.R.; Kerherve, E.; de Araujo, S.G.; and Rocira, A.S., 2011, "Doherty amplifier optimization using robust genetic algorithm and Unscented Transform", Proceedings of Annual IEEE Northeast Workshop CAS, pp. 77-80.
- [8]. Robinson, J.; and Rahmat-Samii, Y., 2004, "Particle swarm optimization in electromagnetic", IEEE Transactions on Antennas and Propagation, 52, no. 2, pp. 397-407.
- [9]. Zaman, M.A.; Gaffar, M.; Alam, M.M.; Mamun, S. A.; and Abdul Matin, M., 2011, "Synthesis of antenna arrays using artificial

bee colony optimization algorithm”, International Journal of Microwave and Optical Technology, 6, no. 8, pp. 234-241.

[10]. Sallem, A.; Benhala, B.; Kotti, M.; Fakhfakh, M.; Ahaitouf, A.; and Loulou, M., 2013, “Application of swarm intelligence techniques to the design of analog circuits: evaluation and comparison”, Analog Integrated Circuits and Signal Processing, 75, no. 3, pp. 499-516.

[11]. Chakraborty M., 2012, “Artificial Neural Network for Performance Modeling and Optimization of CMOS Analog Circuits”, International Journal of Computer Applications, 58, no.18, pp. 6-12.

[12]. Wang, Z.; Luo, X.; and Gong, Z., 2018, “Application of Deep Learning in Analog Circuit Sizing”, Proceedings of the 2018 2nd International Conference on Computer Science and Artificial Intelligence, pp. 571-575.

[13]. Zhang, S.; Lyu, W.; Yang, F.; Yan, C.; Zhou, D.; and Zeng, X., 2019, “Bayesian Optimization Approach for Analog Circuit Synthesis Using Neural Network”, Proceedings of the conference on Design, Automation & Test in Europe, pp. 1-6.

[14]. Massara, R.E., 1991, Optimization Methods in Electronic Circuit Design, Longman Scientific & Technical, Harlow.

[15]. Brayton, R.K.; Hachtel, G.D.; and Sangiovanni-Vincentelli, A.L., 1981, “A survey of optimization techniques for integrated-circuit design”, Proceedings IEEE, 69, no. 10, pp. 1334-1362.

[16]. Ruehli, A.; Sangiovanni-Vincentelli, A.; and Rabbat, G., 1982, “Time Analysis of Large-Scale Circuits Containing One-Way Macromodels”, IEEE Trans. Circuits Syst., CAS-29, no. 3, pp. 185-191.

[17]. Rizzoli, V.; Costanzo, A.; and Cecchetti, C., 1990, “Numerical optimization of broadband nonlinear microwave circuits”, Proceedings of IEEE MTT-S International Symposium, 1, pp. 335-338.

[18]. Ochotta, E.S.; Rutenbar, R.A.; and Carley, L.R., 1996, “Synthesis of high-performance analog circuits in ASTRX/OBLX”, IEEE Transactions on Computer-Aided Design of Integrated Circuits, 15, no. 3, pp. 273-294.

[19]. Zemliak, A., 2001, “Analog System Design Problem Formulation by Optimum Control Theory”, IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, E84-A, no. 8, pp. 2029-2041.

[20]. Pytlak, R., 1999, Numerical Methods for Optimal Control Problems with State Constraints, Springer-Verlag, Berlin.

[21]. Zemliak, A., 2002, “Acceleration effect of system design process”, IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences, E85-A, no. 7, pp. 1751-1759.

[22]. Rouche, N.; Habets, P.; and Laloy, M., 1977, Stability Theory by Lyapunov’s Direct Method, Springer-Verlag, New York.

[23]. Massobrio, G.; and Antognetti, P., 1993, Semiconductor Device Modeling with SPICE, Mc. Graw-Hill, Inc., New York.