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Threshold Logic Gate Family and Implementation of a BCD to7-segment Display

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ABSTRACT
Single Electron tunneling devices (SEDs) and Threshold Logic Gates (TLGs)both have the capabilities of controlling the transport of an electron through a tunnel junction at a particular time. A single electron bearing the charge is adequate to store an information in a SED. The processing delay of Threshold Logic Gates is very low and speed of the processing of TLG based devices will be close to speed of an electron. For implementing logic gates andBCD to 7-segment converter, TLG would be a best candidate to fulfill the necessities. When an Ultra-low noise is thought of, TLG based circuits can the best selection for implementing the desired tunneling circuits. Different TLGs like 2-input AND, 2-input OR, 3-input AND/NAND, 3-input OR/NOR, XOR/XNOR, have been implemented with the help of the concept of linear threshold logic gate. Truth tables or simulated results for them are provided in parallel in due places.

Key words: Tunnel-circuit, Coulomb-blockade, linear threshold gates, processing time

I. INTRODUCTION

Single Electron tunneling based device is one of such an equipment by which all Boolean logic gates and more complex circuits can be implemented. Tunneling events happen when a single electron can pass through the tunnel junction under the action of bias voltage and multiple input voltages connected to the islands via small capacitors. For implementing a BCD to 7-segment converter, TLG would be a suitable candidate.

II. A TUNNEL JUNCTION WITH A TRUE CAPACITOR

The Tunnel Junction-Capacitorset, depicted in Fig.1, is made up of a tunnel junction capacitor C_j and a true capacitor C_c in series. An island represented by a small circle lies between the tunnel junction and the true capacitor. We refer to an island as a circuit node bearing k additional electrons. Only electrons can be removed from or added to the island when tunnel events happen through the tunnel junction. If k = 0, i.e., there is no charge on the island, which indicates in reality that the island has as many protons as it contains electrons, i.e., it is in electrical equilibrium. A negative value of k implies that, k electrons are removed from the island. Since the electron contains a negative charge$q_e = -1.602 \times 10^{-19}$C, then k< 0 implies that a positive charge is present on the island. Similarly when $k > 0$, it implies that electrons are added to the island, i.e., a negative charge is present on the island.

We can express the critical voltage V_c for the tunnel junction[8,9]:

$$V_C = \frac{e}{2(C_C + C_j)} \quad \text{(1a)}$$

We have accepted the sign convention displayed by Fig.1, then the voltage V_j across the tunnel junction is:

$$V_j = \frac{C_c V_{in}}{C_C + C_j} + \frac{ke}{C_C + C_j} \quad \text{(1b)}$$

In Equation (1b), the first term is for the cause of capacitive division of the input voltage V_{in} over the capacitances C_C andC_j.And the second term is the voltage resulting from k additional electron charges present on the island, divided by the total capacitance $(C_C + C_j)$ between the island and ground.

The output voltage V_{out} of Fig.1 the can be defined as below:

$$V_{out} = \frac{C_j V_{in}}{C_C + C_j} - \frac{ke}{C_C + C_j} \quad \text{(1c)}$$

The circuit will remain in a stable state provided that $|V_j| < V_C$is satisfied, and which can be translated with the help of proper substitutions from equations (1a) and (2b) into the following relation:

$$\frac{-e-2ke}{2C_c} < V_{in} < \frac{e-2ke}{2C_c} \quad \text{(1d)}$$

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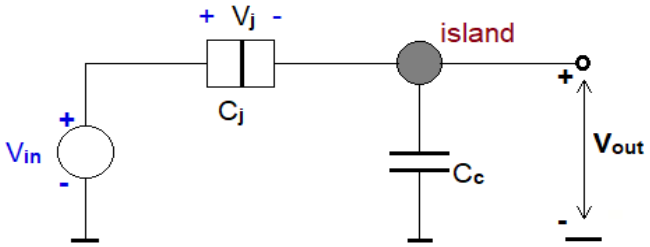

Fig. 1 A Tunnel-junction and a capacitance

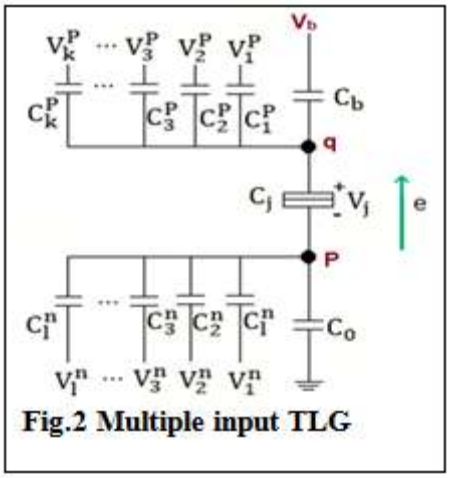

Fig.2 Multiple input TLG

So, for any value of supply voltage V_{in}, the circuit will reach a stable state for a unique value of ksatisfying the above relation (1d). With starting from a stable state, the input voltage of the circuit V_{in} is gradually being increased or decreased, we will initially observe that a similar increase or decrease of the output voltage owing to the capacitive division in Fig.1. However, the voltage V_j acrossthejunctionwouldreachthepointin whichitsabsolute valueislargerthen V_C,as a result anelectronwillpassthroughthejunctiontowardstheside havingthehighestvoltage.At this point,forapositiveinputvoltageV_{in},theelectronmusttun nelawayfrom theisland,givinga suddenincreaseoftheisland'svoltage. Similarly, foranegativeinputvoltageV_{in},theelectronmusttunnel towardsthe island,givingasudden decreaseinthevoltage of the island.

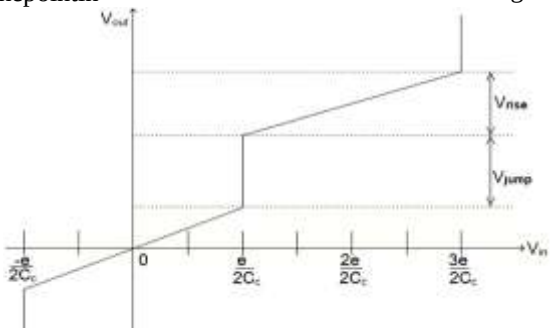

Fig.2 Junction characteristics of tunnel-junction

Thetransfer characteristics of the circuitdisplayedin Fig. 2. In thisfigure,werefer tothe suddenchangeinthe output voltage as $V_{jump} = \frac{e}{C_C + C_j}$ and to the voltage part of V_{in} that is capacitively divided over C_c on the complete input voltage range corresponding to a stable state as $V_{rise} = \frac{eC_j}{(C_C + C_j)C_C}$. It is considered that the ratio of V_{jump} over V_{rise} is $\frac{V_{jump}}{V_{rise}} = \frac{\frac{e}{C_C + C_j}}{\frac{eC_j}{(C_C + C_j)C_C}} = \frac{C_c}{C_j}$, the transfer

function of this circuit is shown in Fig. 2 as a staircase when $V_{jump} >> V_{rise}$ i.e., $C_c >> C_j$.

III. MULTIPLE INPUT THRESHOLD LOGIC GATE

Amultiple threshold logic gate [1, 2, 3, 4, 9, 10] shown in Fig. 3is made up of a tunnel junction having capacitance C_j andresistanceR_j, two multiple input-signals V_k^Ps and V_l^ns connected at two points 'q' and 'p'. where each input voltage $V_k^P$is connected to the point "q" through their corresponding capacitors C_k^Ps; and each input voltage V_l^n, is connected to the point "p" through their respective capacitors C_l^ns. The supply voltage or Bias voltage V_b is connected to the point"q" through a capacitor $C_b$also. Junction capacitor C_j is connected to point "p" whichis connected to the ground through capacitor C_0. LTGs can be implemented with the help of a function presented by the signun function of h(x) expressed by equations (2a) and (2b).

$$g(x) = \mathrm{sgn}\{h(x)\} = \begin{cases} 0, & \text{if } h(x) < 0 \\ 1, & \text{if } h(x) \geq 0 \end{cases} \quad \text{(2a)}$$

$$h(x) = \sum_{k=1}^{n} (w_k \times x_k) - \theta \quad \text{(2b)}$$

where $x_k$being the n-Boolean inputs and w_k being their corresponding n integer weights.

The LTG compares the weighted sum of the inputs $\sum_{k=1}^{n}(w_k \times x_k)$ with the threshold valueθ.When the weighted sum-value is greater than or equal to the critical voltage or threshold value θ then the logic output of the LTG will be high (logical "1"), otherwise it refers to a low (logical "0").

Two basic circuit elements in a LTG being the tunnel junction capacitance $C_j$and the capacitance C_0 areconnected in series. The input signal voltages $V_1^P, V_2^P, V_3^P, \ldots, V_k^P$, which are weighted by their corresponding vector capacitances$C_1^P, C_2^P, C_3^P, \ldots, C_k^P$, are added to the junction voltage,V_j. In contrast, the input signal voltages$V_1^n, V_2^n, V_3^n, \ldots, V_l^n$ weighted by their correspondingvector capacitances $C_1^n, C_2^n, C_3^n, \ldots, C_l^n$, are being subtracted from the voltage, V_j.

The critical voltage $V_c$is indeed required to enable tunneling action, and which acts as the intrinsic threshold of the tunnel junction circuit. The supply or bias voltage $V_b$connected to tunnel junction through the capacitance, C_b, is being used to adjust the gate threshold to the desired valueθ. A tunneling event happens though the tunnel junction, only when an electron passes through the junction from p to q as directed by a green arrow in Fig. 3.

The following notationswe will use for the rest our discussion.

$$C_\Sigma^P = C_b + \sum_{k=1}^{g} C_k^P \quad \text{(3)}$$

$$C_\Sigma^n = C_0 + \sum_{l=1}^{h} C_l^n \quad \text{(4)}$$

$$C_T = C_\Sigma^P C_j + C_\Sigma^P C_\Sigma^n + C_j C_\Sigma^n \quad \text{(5)}$$

Whenever all voltage sources in Fig. 3 are connected to ground, the circuit can be thought of as it is made up of three capacitors namely, C_Σ^P, C_Σ^n and C_j, connected in series. C_T istaken to be the sum of all 2-term products of these three capacitances C_Σ^P, C_Σ^n and C_j.

Now we are to find outthe expression as to the critical voltage V_c of the tunnel junction. We may take the capacitances of the whole circuit as: (i) the capacitance of the tunnel junction to be C_j and(ii) the remaining part of the circuit has the equivalent capacitance to C_e, as observed from the point of view of tunnel junction, we can measure the threshold orcritical voltage [1, 2, 3, 9,10] for the tunnel junction as below.

$$V_c = \frac{e}{2(C_j + C_e)} \quad \text{(6)}$$

$$= \frac{e}{2[C_j + (C_\Sigma^P || C_\Sigma^n)]}$$

$$= \frac{e}{2\left[C_j + \frac{(C_\Sigma^P) * (C_\Sigma^n)}{(C_\Sigma^P + C_\Sigma^n)}\right]}$$

$$= \frac{e(C_\Sigma^P + C_\Sigma^n)}{2[C_j * (C_\Sigma^P + C_\Sigma^n) + (C_\Sigma^P) * (C_\Sigma^n)]}$$

$$= \frac{e(C_\Sigma^P + C_\Sigma^n)}{2C_T} \quad \text{(7)}$$

Given that the voltage of the junction is V_j , a tunneling event comes to happen through this tunnel junction if and only if the condition given below is satisfied.

$$|V_j| \geq V_c \quad \text{(8)}$$

It is decided that if the junction voltage is less than the critical voltage i.e. $|V_j| < V_c$, then there will be no tunneling event through the tunnel junction. As a consequence, the tunneling circuit remains in a stable state.

We can also write for thefunction h(x) as[9,10]

$$C_T h(x) = C_\Sigma^n \sum_{k=1}^{g} C_k^P V_k^P - C_\Sigma^P \sum_{l=1}^{h} C_l^n V_l^n - 0.5\big(C_\Sigma^P + C\Sigma ne + C\Sigma nCbVb \quad \text{(9)}$$

$$h(x) = C_\Sigma^n \sum_{k=1}^{g} C_k^P V_k^P - C_\Sigma^p \sum_{l=1}^{h} C_l^n V_l^n - \theta \quad \text{(10)}$$

and $\theta = 0.5(C_\Sigma^P + C_\Sigma^n)e - C_\Sigma^n C_b V_b$ ....(11)

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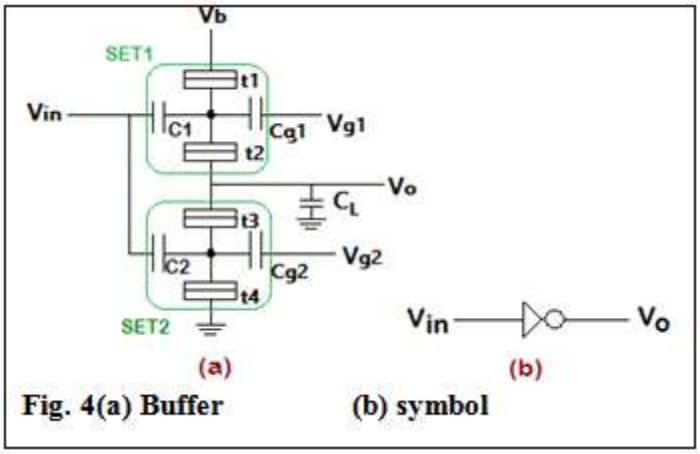

Fig. 4(a) Buffer (b) symbol

IV. BUFFER

The buffer or inverter [2, 3, 4, 8, 9, 10] complementing its own input is depicted in Fig. 4(a) which is made up of two single electron transistors (SETs) connected in series. The two input voltages of same values are directly coupled to the islands of the SET1 and SET2 [1, 2, 3, 9, 10] through two capacitors C_1 and C_2having the same values. The islands of the both SETs have the sizesof 10 nm diameter of gold and their capacitances should be less than 10^{-17} F. The output terminal $V_0$is connected to the channel between SET1 and SET2 and to the ground through a capacitor$C_L$for the purpose of putting down charging effects.

For the buffer, the parameter values chosen are:V_{g1}=0, V_{g2}=0.1× $\frac{q_e}{C}$, $C_L = 9C$, $t_4 = \frac{1}{10}C$, $t_3 = \frac{1}{2}C$, $t_2 = \frac{1}{2}C$, $t_1 = \frac{1}{10}C$, $C_1 = \frac{1}{2}C$,$C_2 = \frac{1}{2}C$,$C_{g1} = \frac{17}{4}C$ and $C_{g2} = \frac{17}{4}C$, R1 =R2=50KΩ. For simulation purpose, the value of C will be taken as 1aF.

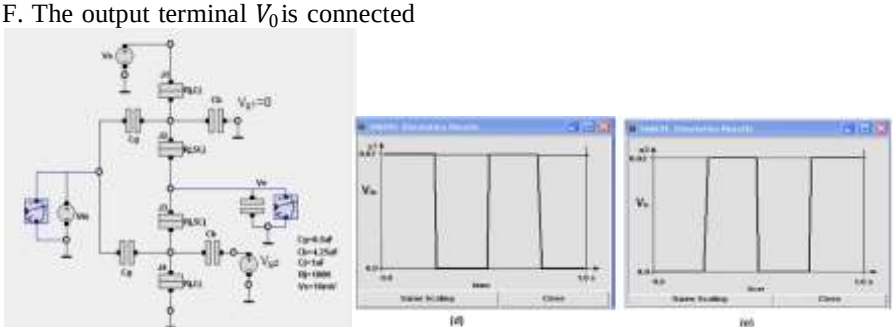

Fig. 4(c) Simulation set of BufferFig.4 (d), (e) Simulation result of Buffer input and output

The operation of the buffer will be as: - the output V_0value will be high till the input voltage V_{in} is low and the V_0value will be low whenever the input voltage is high. Inobtaining this target, we must set the voltages for $V_{g1} = 0\ V$ andV_{g2}=16mV along with the tuning gate voltages, at present, V_{in} both for SET1 and SET2. SET1 is in conduction mode if V_{in} is set to low and the SET2 is in Coulomb blockade [2, 3, 4, 5, 6,11]. This connects the output voltage V_0 to V_b and therefore the output voltage becomes high.Coulomb blockade impedes the steady flow of current, as the high voltage (logic 1) is applied to the input terminal(s), it causes the induced charge on each of the islands of the SET1 and SET2to shift by a fraction of an electron charge and necessitates the SET1 in Coulomb blockade and the SET2 in conducting mode. So, the output shifts from high to low (logic 0).

In this work, we have assumed the Boolean logic inputs "0" =0 Volts and logic "1"=0.1× $\frac{q_e}{C}$.

For simulation and other purposes, we will consider that C=1aF and Logic "1"= 0.1× $\frac{1.602\times10^{-19}}{1\times10^{-18}}$=0.1 × 1.602 × 10^{-2}=16.02 × 10^{-3} =16.02 ≅ 16 mV.

V. THRESHOLD LOGIC EQUATION FOR OR GATE

Consider the threshold logic equation of OR gate is OR(A,B)=sgn{$w_A.A + w_B.B - \theta$}.To make the threshold logic OR gate, we draw the Table-4 of OR gate and compare the weights of variables w_A

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and w_B of two variables A and B respectively with the threshold value θ.

Table-4

A	B	F(A,B)	θ	Eqn. no.
0	0	0	$0<\theta$	(1)
0	1	1	$w_B \geq \theta$	(2)
1	0	1	$w_A \geq \theta$	(3)
1	1	1	$w_B + w_A \geq \theta$	(4)

For the 4 equations in Table-4, if we assume w_B=1, w_A=1 and θ=0.5, then all the 4 equations are satisfied. Hence the Threshold logic equation for OR gate is given in equation (12) and its corresponding threshold logic gate is drawn in Fig. 5(a)

$$OR(A,B) = sgn\{A + B - 0.5\} \cdots\cdots\cdots (12)$$

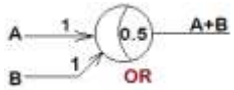

Fig. 5(a) Threshold logic OR gate

For implementing the OR gate we shall use the parameters $C_1^n = C_2^n$=0.5aF, $C_3 = 11.7aF, C_{b1} = C_{b2} = 4.25aF$, $C_{g1} = C_{g2} = 0.5aF, C_L = 9aF, C_0 = 8aF$, R_j=$10^5\Omega$, $V_s = 16mV$ in Fig. 5(a) and accordingly after running the simulator the output we get is given in Fig. 5(b)-(e).

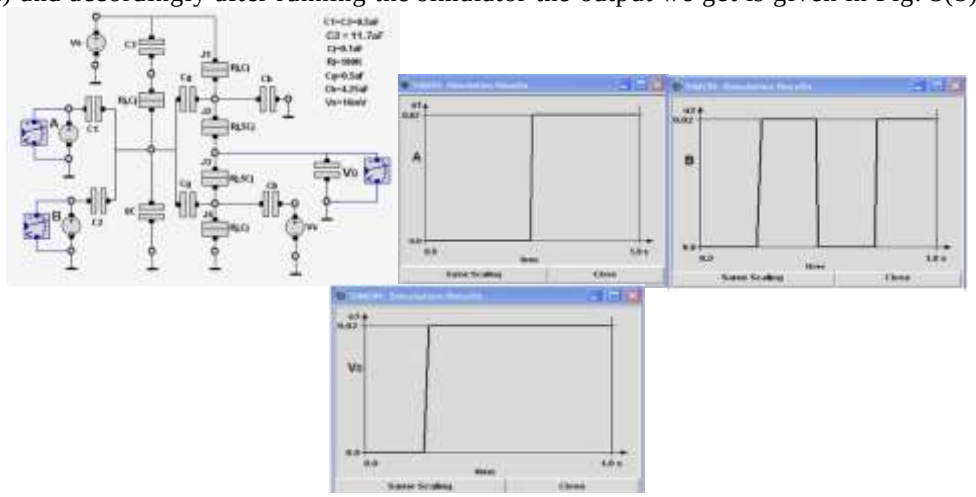

Fig. 5(b) OR gate (c) (d) (e)

Fig. 5(c)-(e) simulation result of OR gate

For the case of NOR

As we know that buffer inverts itself i.e., inverts its own input signal, we modify the threshold equation of OR(A, B) such that it determines NOR(A,B). So when we combine the result of OR(A,B)with a buffer or inverter, a new threshold logic buffered gate, we get, that gives us the value of NOR (A, B) and the equation of the NOR logic gate will be

NOR (A, B) =$\overline{OR(A,B)}$

$$= sgn\{-A - B - (-0.5)\} \cdots\cdots (13)$$

Here the value of the threshold voltage -0.5 may be any value in the range of $-1 > \theta \geq 0$.

Table-5

A	B	$\{w_A + w_B\}$	$\theta = -0.5$	$F(A,B)$
0	0	0	$0 \geq -0.5$	1
0	1	-1	$-1 < -0.5$	0
1	0	-1	$-1 < -0.5$	0
1	1	-2	$-2 < -0.5$	0

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From the Table -5 it is observed that F (A, B) satisfies all the conditions of an NOR gate, so the equation (13) we have is correct. Simulation set and simulation result are given in Fig, 6(a) and 6(b) respectively.

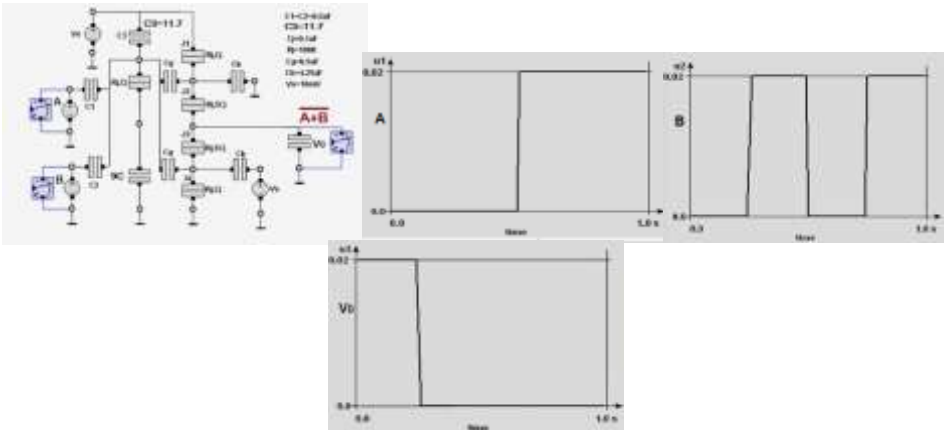

Fig 6(a) TLG based NOR gate Fig, 6(b) Simulation result of NOR gate

For implementing the buffered Boolean logic NOR gate we will use the parameters logic input "0"=0V, logic "1" = 16mV, $C_1^n = C_2^n$=0.5aF,$C_3 = 11.7aF, C_b = C_{b1} = C_{b2} = 4.25aF, C_{g1} = C_{g2}$ =0.5aF, $C_L = 9aF, C_0 = 9aF$, $R_j = 10^5\Omega, V_s = V_b$ =16mVand accordingly after simulation the result we have is given in Fig. 6(b).

VI. 2-INPUT AND GATE

For making the threshold logic gate of 2-input AND gate, we can draw the Table-6of an AND gate and compare the weights of variables w_A and w_B of two variables A and B respectively with the threshold θ [1,2,3,4].

Table-6

A	B	F(A,B)	θ	Eqn. no.
0	0	0	0<θ	(1)
0	1	0	$w_B < \theta$	(2)
1	0	0	$w_A < \theta$	(3)
1	1	1	$w_B + w_A \geq \theta$	(4)

After solving the 4 equations in 4th column of Table 6, we get one set of solution w_B=1, w_A=1 and θ=2. So the Threshold logic equation for AND gate is given in equation (14) and its corresponding threshold logic gate is drawn in Fig. 7(a)

$AND(A,B) = sgn\{A + B - 2\}$ ..... (14)

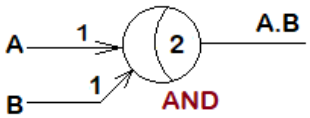

Fig. 7(a) Threshold logic AND gate

For implementing the AND gate we will use the parameters $C_1^n = C_2^n = 0.5aF, C_{b1} = C_{b2} = 4.25aF, C_{g1} = C_{g2} = 0.5aF, C_L = 9aF, C_0 = 8aF$, $R_j = 10^5\Omega$.The simulation set is given in Fig. 7(b) and after simulating the result we get is given in Fig. 7(c).

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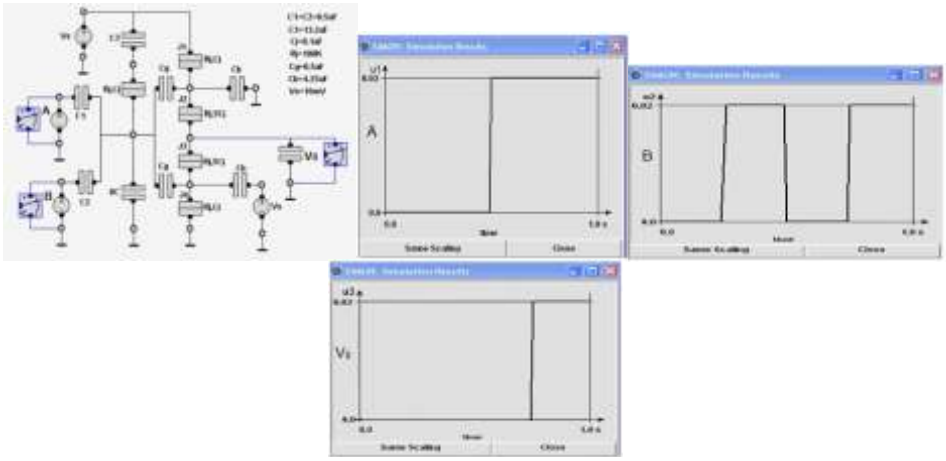

Fig.7 (b) AND Gate (c) (d) (e)

Fig.7 (d), (e) Simulation result of 2-input AND gate

A	B	C	F(A,B,C)= ABC	θ
0	0	0	0	0<θ
0	0	1	0	$\theta > w_C$
0	1	0	0	$\theta > w_B$
0	1	1	0	$\theta > w_B + w_C$
1	0	0	0	$\theta > w_A$
1	0	1	0	$\theta > w_A + w_C$
1	1	0	0	$\theta > w_A + w_B$
1	1	1	1	$w_A + w_B + w_C \geq \theta$

VII. THRESHOLD LOGIC EQUATION FOR 3-INPUT AND GATETABLE-7

As AND gate is a positive logic we shall assume that all the values of w_A, w_B, w_C andθ are positive. If we take $w_A = 1, w_B = 1$,w_C=1 and$\theta = 2.5$ (or any value in the range $2 <\theta\leq 3$), then all the conditionalequations in the 5th column inTable-7 are satisfied. So the threshold logic equation for 3-input AND gate is

$AND(A,B,C) = sgn\{A + B + C - 2.5\}$ ····· (15)

In the same way, we can obtain a solution set for 3-input NAND gate,$w_A = -1$, $w_B = -1$,$w_C = -1$ and$\theta = -2.5$. So, the corresponding threshold logic gate will be

NAND (A,B,C) $= sgn\{-A - B - C - (-2.5)\}$ ····· (16)

Simulation set and simulation result are given in Fig. (8a) and 8(b) (in septate page).

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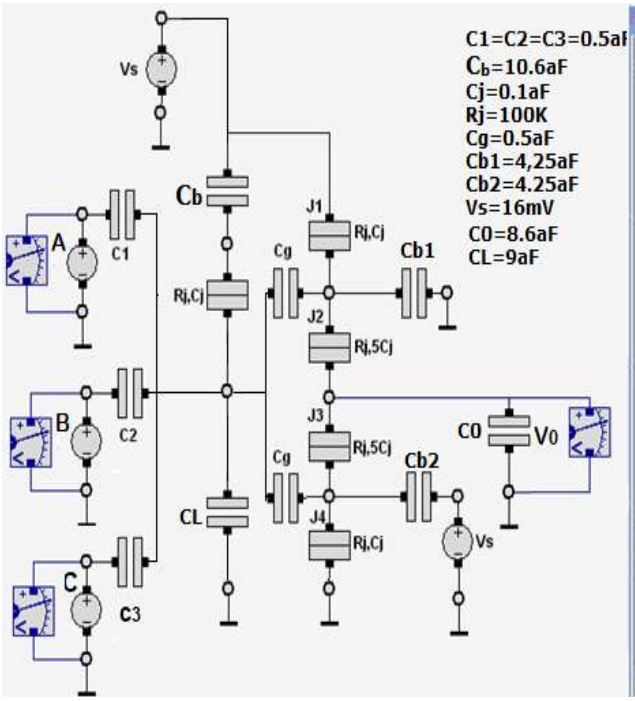

Fig. 8(a) Simulation set of 3-input AND gate

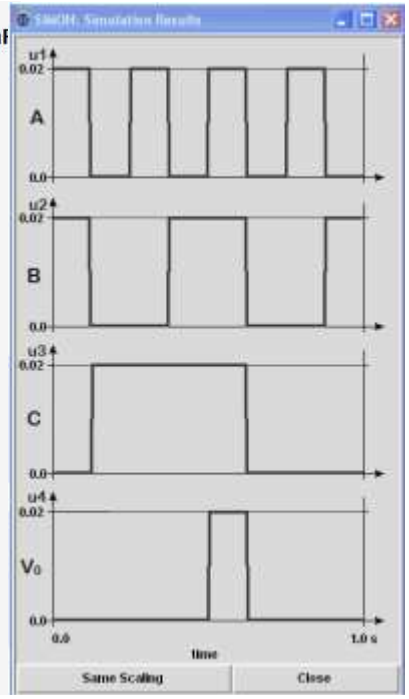

Fig. 8(b) Simulation result of 3-input AND gate

VIII. XOR GATE

The logic function of XOR gate is defined as Y=A.$\bar{B}$ +$\bar{A}$.B, where A and B are two variables. Space plot diagram of Y in 2D space is shown in Fig. 9. From this, we observe that no linear separating line that is separating the green and colorless bubbles can be drawn. So One can decide that the Boolean logic function is not linearly separable . Therefore we would not be able to draw a threshold logic gate that represents the equation Y =A.$\bar{B}$ +$\bar{A}$.B.

Now for representing the Boolean function Y =A.$\bar{B}$ +$\bar{A}$.B by a threshold logic gate, first we express P = (A.$\bar{B}$) with the help of threshold gate-based equation as given in equation (17).

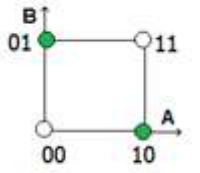

Fig. 9 Space plot of Y= $\bar{A}$B+A$\bar{B}$

P = $sgn\{A + \bar{B} - 2\}$ ..... (17)

As we know B + $\bar{B}$ =1 or $\bar{B}$= − B + 1, the equation (17) can be written as equation (18).

P = $sgn\{A - B - (1)\}$ ..... (18)

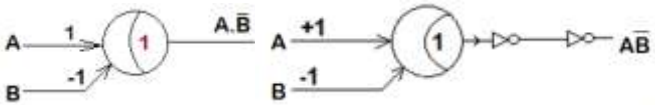

Fig. 9(a) Threshold gate of P = A.B

Fig. 9(b) Threshold gate of A .$\bar{B}$ using 2-buffers

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Table-8
Truth table of equation (18)

A	B	P
0	0	0
0	1	0
1	0	1
1	1	0

Table-9
Truth table of $\bar{P}$

A	B	P	θ
0	0	1	$0 \geq \theta$
0	1	1	$w_b \geq \theta$
1	0	0	$w_a < \theta$
1	1	1	$w_a + w_b \geq \theta$

Truth table of equation (18) Truth table of $\bar{P}$

We can modify the threshold equation of P as we know that the buffer inverts its input signal, so it calculates $\bar{P}=\bar{A}+B$ or $\bar{P}=\text{sgn}\{-A+B-(-0.5)\}$ and its corresponding truth table is given in Table-9.

For implementing the threshold logic gate of $\bar{P}$ we require the logic input "0"=0V, logic "1" = 16mV,C=1aF, $C_1^n = C_1^P = \frac{1}{2}C$ =0.5aF, $C_b = 10.24aF$, $C_j = 0.25aF$, $C_L = 9aF$, $C_0 = 9.5aF$, R_j=$10^5\Omega$,. $V_b = 0.95\, e/C = 15.2mV$ $(as\ e/C = 160mV)$which is close to 16mV, so V_b =V_s=16mV.

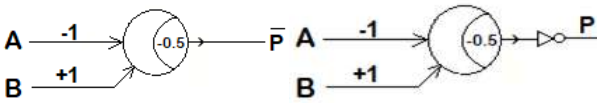

Fig. 10 (a) Threshold logic gate of $\bar{P}$ (b) of P

Now we are to express the Boolean expression $Y=A.\bar{B}+\bar{A}.B$. We assume $P=\bar{A}.B$, So $Y=A.\bar{B}+\bar{A}.B = P + \bar{A}.B$.

$$Y = P + \bar{A}.B \quad \cdots\cdots (18a)$$

For finding out the threshold gate logic of equation (18a), we draw the truth Table-10 with the assistance of Table-8, and from Table-10we solve the equations to get the weight values in 5th col. of Table-10.

Table-10

A	B	P	Y	θ
0	0	0	0	$0<\theta$
0	1	0	1	$W_2 \geq \theta$
1	0	1	1	$W_1 + W_3 \geq \theta$
1	1	0	0	$W_1 + W_2 < \theta$

After solving the conditional equations in Table-12, we obtain a solution set $\{W_1, W_2, W_3; \theta\}$ = {-1, 1, 2 ; 1}.

Hence the Threshold equation for the Y or an for XOR is

$$Y = \text{sgn}\{-A + B + 2P - (1)\} \quad \cdots\cdots (19)$$

And its corresponding Threshold logic gate is depicted in Fig. 11**.** For correct operation, we are to apply a buffer in series to obtain an XNOR which is also shown in Fig. 11. If we again add another buffer in series we obtain an XOR gate shown in Fig. 11 as well.

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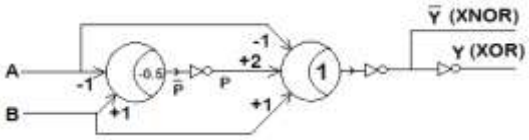

Fig. 11 XOR/ XNOR gate of two inputs

IX. FOR FINDING OUT THE THRESHOLD CIRCUIT PARAMETERS OF AN XOR / XNOR GATE WE DESCRIBE THE FOLLOWING APPROACH:

Y = sgn $\{-A + B + 2P - (1)\}$ ..... (19)

Comparing equation (10) ,(11) and (19), we observe the following relation for the weights

$2C_{\Sigma}^{p} C_1^n = 2C_{\Sigma}^{n} C_1^P = C_{\Sigma}^{n} C_2^P$

Assuming $C_{\Sigma}^{P} = C_{\Sigma}^{n}$ then we have

$C_1^n = C_1^P = 0.5C_2^p = \frac{1}{2}C$ (assume)

$Assuming C_{\Sigma}^{P}$=10C, C_{Σ}^{n}=10C, from eqn. (3)

$$C_{\Sigma}^{P} = C_b + \sum_{k=1}^{g} C_k^P$$

10C =C_b + 0.5C+1C $\Longrightarrow$ $C_b = 8.5C$

From equation (4),$C_{\Sigma}^{n} = C_0 + \sum_{l=1}^{h} C_l^n$

10C= C_0 +0.5C $\Longrightarrow$ C_0 =9.5C

Now that we have obtained the ability of the circuit to perform a linear threshold function, we will investigate the contributions of the charges to the output of the circuit V_0. If a charge of 1-electron is passed through the tunnel junction in the direction of the arrow (as shown in in Fig. 3, from p to q), it will have the effect of increasing the charge on node q by -e, which in turn effects onV_q byδV_q,(δq_{charge} = -e) =$\frac{e(C_j+C_{\Sigma}^{n})}{C_T}$. This effect, due to voltage division, will be visible at the output as V_0(δq_{charge} =−e) =$\frac{-e(C_j)}{C_T}$.In the same way, if a net charge of 1 electron is passed through the tunnel junction in the direction of the arrow, it will have the effect of increasing the charge on node p by +e, which in tum effects the output byδV_0(δp_{charge} = e)=$\frac{e(C_j+C_{\Sigma}^{p})}{C_T}$. Concluding electronispassedthroughthetunneljunction in the direction of the arrow,theeffectontheoutputvoltageV_0will be:

δV_0(1e) = V_0(δq_{charge} = -e) + δV_0(δp_{charge} = e)

= $\frac{-e(C_j)+e(C_j+C_{\Sigma}^{p})}{C_T}$ = $\frac{e(C_{\Sigma}^{p})}{C_T}$ ..... (20)

Taking all the parameters as chosen above, we would be able to calculate the effect of the event of the tunneling over the output voltage provided by the equation (20) as below.

∂V$_0$(le)=$\frac{eC_{\Sigma}^{P}}{C_{\Sigma}^{P}C_j+C_{\Sigma}^{P}C_{\Sigma}^{n}+C_jC_{\Sigma}^{n}}$=$\frac{10e}{(10\times0.25+10\times10+0.25\times10)C}$

=$\frac{10e}{105C}$=0.095e/C ..... (21)

Asthe tunneling event effects on the output determines the voltage level of a logic 1 and when there is no tunneling event the output determines the voltage level of a logic 0. So we accept the following signal presentations for two logic signals: logic 1= $0.095e/C \cong 0.1e/C$ Volt and logic 0 = 0 Volt.

As the voltage logic levels representation and the weights corresponding to the input signals are assigned and they are considered to be fixed, we are interested in finding out the proper threshold value θ.

The threshold in the circuit is thought of the critical voltage V_c of the junction. The frequency of the tunnel event is inversely proportional to the difference between the junction voltage $V_j$and the critical voltage V_c $(i.e., V_j \sim V_c)$ which coincides with the value of h(x). Consequently we should accommodate for some margin in the input signals.

For compromising themargin in the input signals and maximizing the value of h(x), we can put the threshold value θ equal to = 1. It is considered that all other parameters or terms associated with, contributing to h(x) are selected in their ratios. We should also use the same ratio for θ. In our convenience, we take the value of$C_{\Sigma}^{n} \times C_2^P$ =1 and the value of $0.095e/C \cong 0.1e/C$ *is* representing the logic value 1. We represent the threshold value θ[7, 8, 9]as per the ratio. i.e.,

$\theta = 1 \times C_{\Sigma}^{n} \times C_2^P \times 0.1e/C$ ..... (22)

Substitute this value to the equationbelow[9].

θ=0.5$\left(C_{\Sigma}^{P} + C_{\Sigma}^{n}\right)e - C_{\Sigma}^{n} C_b V_b$ ..... (23)

The value of C_{Σ}^{n} C_2^P is used to represent the weight of value 1 and the value of $0.095e/C \cong 0.1e/C$ is used to indicate an input logic value equal to 1. Substituting these values to the equation (23)

$1 \times C_{\Sigma}^{n} C_2^P \times 0.1e/C = 0.5\left(C_{\Sigma}^{P} + C_{\Sigma}^{n}\right)e - C_{\Sigma}^{n} C_b V_b$ ..... (24)

$\Longrightarrow$ $1 \times 1 \times 1C \times 0.1e = 0.5(10C + 10C)e - 10C \times C_b V_b$

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$\Longrightarrow V_b$ =0.99e
HenceC_bV_b =8.5C×0.99e/C=0.84e ..... (25)

If we want to take a larger or lesser value of V_b the value of C_b would be inversely increased or decreased as the product of the two equal to 0.84e, i.e. $C_bV_b =$ 0.84e. Given that $C_b = 8.5C$ then V_b =15.81mV
We are to add an additional capacitance C_g between the point q and ground in Fig.3 for balancing the required input voltage(s), satisfying the equation

C_g=8.5C−C_b ..... (26)

After using the parameter's ratio for the above cases, we have verified the design of **XOR**. For the simulation purpose we have taken the values as follows:
the threshold logic gate input logic input "0"=0V, logic "1" = 16mV,C=1aF, $C_1^n = C_1^P = 0.5C_2^p = \frac{1}{2}C$ =0.5aF, $C_b = 8.5aF$, $C_j = 0.25aF$, $C_L = 9aF, C_0 = 9.5aF$, R_j=$10^5\Omega$,. $V_b = 15.81mV$ which is close to 16mV, so V_b =V_s=16mV

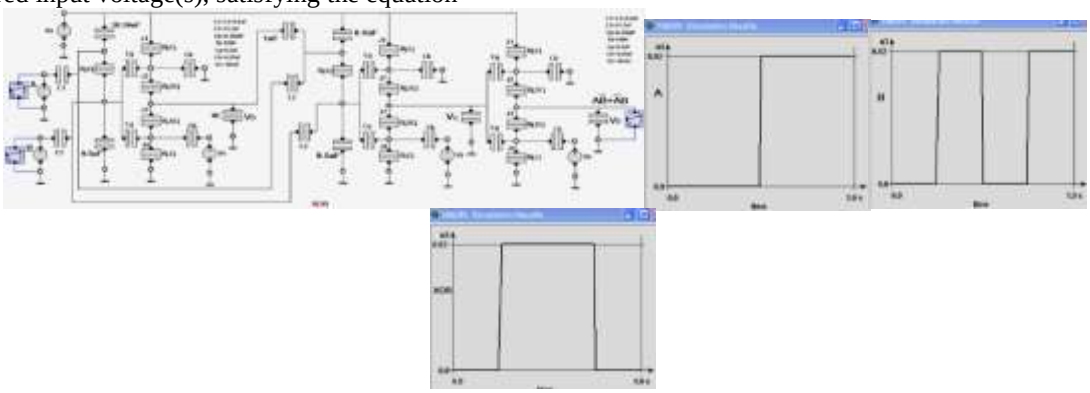

Fig. 12(a) Simulation set of XOR(A,B)Fig.12(b) Simulation result of XOR(A,B)

X. 3-INPUT OR/NOR GATE

Table-11
(3-input OR gate)

A	B	C	F(A,B,C) =A+B+C	θ	Eqn. no.
0	0	0	0	0<θ	(1)
0	0	1	1	$w_C \geq \theta$	(2)
0	1	0	1	$w_B \geq \theta$	(3)
0	1	1	1	$w_B + w_C \geq \theta$	(4)
1	0	0	1	$w_A \geq \theta$	(5)
1	0	1	1	$w_A + w_C \geq \theta$	(6)
1	1	0	1	$w_A + w_B \geq \theta$	(7)
1	1	1	1	$w_A + w_B + w_C \geq \theta$	(8)

For 3-input OR,F(ABC)= A+B+C is a positive input logic gate and we are inspired to assign the coefficient values of $w_A = w_B = w_C$=1.For the sake of the conditional equation 0<θ in the equation of the Table-11, we can take any value in the range $0 < \theta \leq 1$.Taking an integer is fine, hence θ=1. On putting the values of $w_A = w_B = w_C$=1andθ=1 in the 8-equations in Table-11, anybody can observe that all the equations are satisfied. Hence, one solution set is being $\{wa, wb, w3;\ \theta\} = \{1, 1, 1;\ 1\}$ and accordingly the threshold equation of the 3-input OR gate would be:
OR (ABC) = sign $\{1.A + 1.B + 1.C - (\theta)\}$
$=sgn\{A + B + C - (1)\}$ ..... (27)

And the state space solution diagram has been shown in Fig.13(a). The solution points indicating blue small circles have the values equal to 1 of (A+B+C). Clear from the figure that the 3-input OR gate equation is linearly separable, therefore a linear threshold logic gate can be drawn without any hesitation, and its corresponding TLG is depicted in Fig. 13(b)

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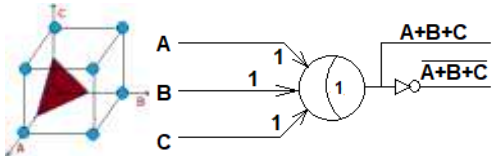

Fig. 13(a) State space diagram of (A+B+C)13(b) 3-in OR/NOR gate

To be informed that for the correct operation of a 3-input OR gate, one have to include an inverter. To do so, connect a 3-in NOR gate and an inverter in series and we will find out a threshold logic equation of that 3-in NOR gate. Consider the Table-12.

Table-12
(3-input NOR gate)

A	B	C	F(A,B,C) $=\overline{A+B+C}$	θ	Eqn. no.
0	0	0	1	0≥θ	(1)
0	0	1	0	$w_C < \theta$	(2)
0	1	0	0	$w_B < \theta$	(3)
0	1	1	0	$w_B + w_C < \theta$	(4)
1	0	0	0	$w_A < \theta$	(5)
1	0	1	0	$w_A + w_C < \theta$	(6)
1	1	0	0	$w_A + w_B < \theta$	(7)
1	1	1	0	$w_A + w_B + w_C < \theta$	(8)

In the Table-12 there are 8 equations. 1st equation tells us that θ must be a non-positive number, consider θ=-0.5. As NOR gate is negative logic, one can take the values of $w_A = w_B = w_C = -1$ and when he/she would put the values to the 8 equations in Table-12, all the equation are satisfied. Hence one solution set is$\{w_A, w_B, w_C ; \theta\} = \{-1, -1, -1 ; -0.5\}$. Depending upon this solution set, the threshold logic equation is provided in equation (28) and its threshold logic gate is depicted in Fig. 13(c).

NOR (ABC) = $sgn\{-1.A - 1.B - 1.C - (-0.5)\}$
$=sgn\{-A - B - C - (-0.5)\}$ ..... (28)

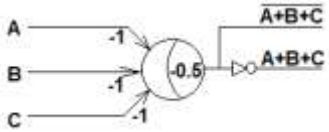

Fig. 13(c) 3-input NOR/OR gate

When we are referring to a logic function such as OR, we will imply the logic function performed by the whole gate (i.e., threshold gate output + buffer).

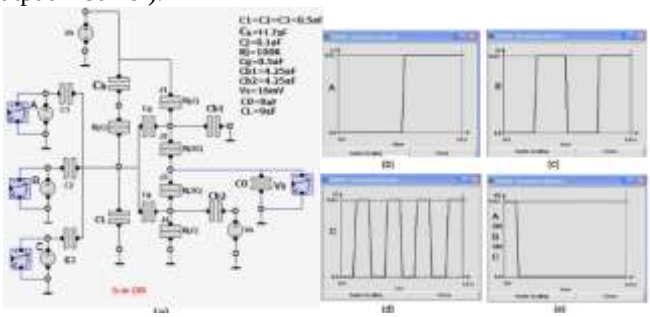

Fig. 14(a) 3-in OR gate; (b), (c), (d) and (f) are simulation results

So, 3-in OR= (3-in NOR + buffer) is to be accepted and is drawn in Fig.14(a) with its simulated waves in Fig. 14(b), (c), (d), and (e). For the purpose of implement a simulation the parameters to be taken is as: logic input

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"0"=0V, logic "1" = 16mV, $C_1^n = C_2^n$=0.5aF,$C_b = 11.7aF, C_b = C_{b1} = C_{b2} = 4.25aF$, $C_{g1} = C_{g2} = 0.5aF, C_L = 9aF, C_0 = 8aF$, R_j=$10^5\Omega, V_s = V_b = 16mV$.

XI. ANALYSIS OF BCD TO 7-SEGMENT DISPLAY

Karnaugh maps of a BCD to 7-segment decoder is given in Fig. 15(a).

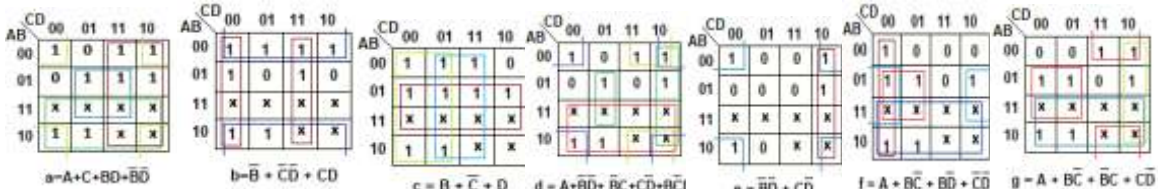

Fig. 15(a) Karnaugh Maps of BCD to 7-segments decoder

Part-1: a= A+C+BD+$\bar{B}\bar{D}$

a= A+C+BD+$\bar{B}\bar{D}$ ..... (29)

The equation (29) is not linear separable as (BD+$\bar{B}\bar{D}$) is an XNOR gate equation which is not linear. For our conveniences, we assume E = (BD+$\bar{B}\bar{D}$), as a result the equation derived, a= A+C+E which is a 3-input OR gate equation. Being combined the XNOR gate and 3-in OR gate in series, we have a threshold network representing equation (29) and it points to the Fig.15 below.

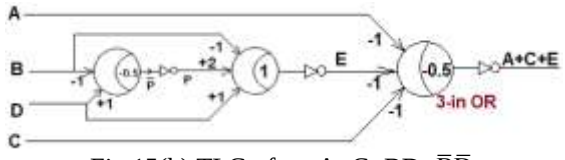

Fig.15(b) TLG of a= A+C+BD+$\bar{B}\bar{D}$

Part 2: b=$\bar{B}$ + $\bar{C}\bar{D}$ +CD

b=$\bar{B}$ + $\bar{C}\bar{D}$ +CD.....(30)

The equation (30) is not linear separable as ($\bar{C}$ $\bar{D}$ +CD) is an XNOR gate equation which is not linear. For our convenient we assume E = ($\bar{C}$ $\bar{D}$+CD), as a result the equation derived, b= $\bar{B}$+E which is a 2-input OR gate equation. Being combined the XNOR gate and 2-in OR gate in series, we have a threshold network representedby the Fig.16 below.

Or

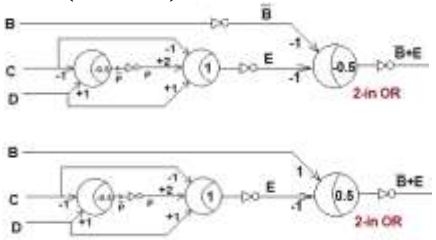

Fig.16 TLG of b=$\bar{B}$ + $\bar{C}\bar{D}$

Part 3: c=B+$\bar{C}$+D

c=B+$\bar{C}$+D……(31)

The equation (31) is linearly separable as (B+$\bar{C}$+D) is a 3-in OR gate equation which is linear. Using a 3-input OR threshold logic gate we will have a threshold network representing equation (27). In our case, we have to modify the threshold logic equation as below:

From equation (31) we can write NOR (B$\bar{C}$D) =$sgn\{-B-\bar{C}-D-(-0.5)\}$. As we know C +$\bar{C}$=1 which implies $-\bar{C}$=C−1.

So, NOR(B$\bar{C}$D) =$sgn\{-B-\bar{C}-D-(-0.5)\}$

= $sgn\{-B+C-D-$

$(0.5)\}$ .....(32)

According to the equation (35), one can draw the threshold logic gate easily and it is given in Fig. 17.

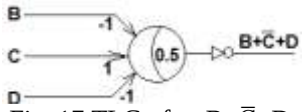

Fig. 17 TLG of c=B+$\bar{C}$+D

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Part 4: d=A+$\bar{B}\bar{D}$+$\bar{B}$C+C$\bar{D}$+B$\bar{C}$D

d=A+$\bar{B}\bar{D}$+$\bar{B}$C+C$\bar{D}$+B$\bar{C}$D……(33)

D is not linearly separable. We can consider the equation as

d= [{A+ ($\bar{B}\bar{D}$+$\bar{B}$C+C$\bar{D}$)} +B$\bar{C}$D]……(34)

Part 4(a)

The sum of product of three variable $\bar{B}$, C and $\bar{D}$ taken two at a time ($\bar{B}\bar{D}$+$\bar{B}$C+C$\bar{D}$) is similar to (xy+yz+zx). Now consider the truth table of (xy+yz+zx) and comparing the threshold conditions we are intended to drawing the Table-13.

Table-13
Truth table of (xy+yz+zx)

Inputs			output	Threshold Condition	Equation No.
x	y	z	(xy+yz +zx)	θ	
0	0	0	0	0<θ	(1)
0	0	1	0	w3< θ	(2)
0	1	0	0	w2< θ	(3)
0	1	1	1	w2+w3≥ θ	(4)
1	0	0	0	w1< θ	(5)
1	0	1	1	w1+w3≥ θ	(6)
1	1	0	1	w1+w2≥ θ	(7)
1	1	1	1	w1+w2+w3≥ θ	(8)

In the above threshold conditional equation from (1) through (8) in the Table-13, if we take w_1=w_2=w_3=1 and $\theta = 2$ then all the conditional equations are satisfied. So the threshold logic equation is

$f(xyz) = sgn\{w_1.x + w_2.y + w_3.z-(\theta = 2)\}$

$f(xyz)= sgn\{x + y + z - (2)\}$……(35)

Complement of $f(xyz)$ is

$\bar{f}(xyz) = sgn\{w_1.x + w_2.y + w_3.z-(\theta)\}$……(36)

Table-16
Truth table of (xy+yz+zx)

Inputs			output	Threshold Condition	Equation No.
x	y	z	$\overline{xy+yz+zx}$	θ	
0	0	0	1	0≥ θ	(1)
0	0	1	1	w3≥ θ	(2)
0	1	0	1	w2≥ θ	(3)
0	1	1	0	w2+w3< θ	(4)
1	0	0	1	w1≥ θ	(5)
1	0	1	0	w1+w3< θ	(6)
1	1	0	0	w1+w2< θ	(7)
1	1	1	0	w1+w2+w3< θ	(8)

As $\bar{f}(xyz)$= gate is negative logic, one can take the values of $w_A = w_B = w_C = -1$ and $\theta = -1.5$, when he/she would put the values to the 8 equations in Table-16, all the equation are satisfied. Hence one solution set is $\{w_A, w_B, w_C ; \theta\} = \{-1, -1, -1 ; -0.5\}$.

$\bar{f}(xyz)$ = $sgn\{-1.x - 1.y - 1.z - (-1.5)\}$

$=sgn\{-x - y - z - (-1.5)\}$……(37)

Instead of variables x, y and z if we can take $\bar{B}$, C and $\bar{D}$, then the equation (37) is converted to.

$\bar{f}(\bar{B}C\bar{D})=sgn\{-\bar{B} - C - \bar{D} - (-1.5)\}$

$= sgn\{B - 1 - C + D - 1 - (-1.5)\}$since B+$\bar{B}$=1]

$= sgn\{B - C + D - (0.5)\}$……(38)

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Following the equation (38), we will be able to implement the threshold logic gate of X = ($\bar{B}\bar{D}$+$\bar{B}$C+C$\bar{D}$) which is given in Fig. 18(a).

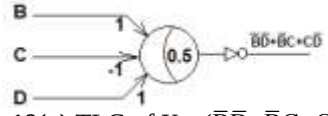

Fig. 18(a) TLG of X= ($\bar{B}\bar{D}$+$\bar{B}$C+C$\bar{D}$)

Part 4(b)

In equation (34),d=[A+($\bar{B}\bar{D}$+$\bar{B}$C+C$\bar{D}$)+(B$\bar{C}$D)], we take the factor B$\bar{C}$D which is a 3-input AND Boolean function.

As we are to find out the complement of 3-input AND gate, we can take the equation (16)

NAND(ABC)=$\overline{AND(A,B,C)}$=$sgn\{-A-B-C+2.5\}$

$=sgn\{-A-B-C-(-2.5)\}$ ..... (16)

Instead of variables A, B and C we replace them by B, $\bar{C}$ and D, hence we get

NAND(B$\bar{C}$D)= $sgn\{-B-\bar{C}-D-(-2.5)\}$

$=sgn\{-B+(C-1)-D-(-2.5)\}$

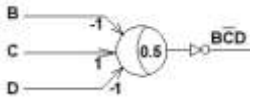

Fig. 18(b) TLG of Y = B$\bar{C}$D

$=sgn\{-B+C-D-(-1.5)\}$ .....(39)

Following the equation (39), we will be able to implement the threshold logic gate of Y = B$\bar{C}$D which is given in Fig. 18(b).

Now the equation (34) can be written as d=A+X+Y which can be visualized as a 3-input OR gate given in Fig. 13(b). With the help of the Fig. 18(a), Fig.18(b) and Fig. 13(b), we can construct the threshold logic gate of d=A+X+Y ord=[A+($\bar{B}\bar{D}$+$\bar{B}$C+C$\bar{D}$)+(B$\bar{C}$D)] and this Figure is placed in in Fig. 19.

Part4(c)

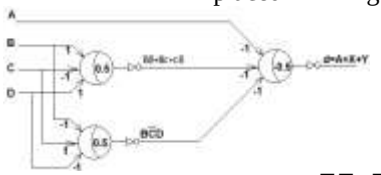

Fig. 19 threshold logic gate of d=A+X+Y= [A+($\bar{B}\bar{D}$+$\bar{B}$C+C$\bar{D}$)+(B$\bar{C}$D)]

Part 5: e=$\bar{B}\bar{D}$+C$\bar{D}$=($\bar{B}$+C)$\bar{D}$ .....(40)

The function **e=$\bar{B}\bar{D}$+C$\bar{D}$ = ($\bar{B}$+C)$\bar{D}$** is linearly separable when we observe from the space diagram given in Fig. 20. Truth table is given in Table-15,

Table-15

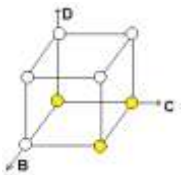

Fig. 20 space plot diagram of **e=$\bar{B}\bar{D}$+C$\bar{D}$**

Table-15

B	C	D	BD+CD	Threshold θ	Eqn. no.
0	0	0	1	$0 \geq \theta$	(1)
0	0	1	0	$w3 < \theta$	(2)
0	1	0	1	$w2 \geq \theta$	(3)
0	1	1	0	$w2+w3 < \theta$	(4)
1	0	0	0	$w1 < \theta$	(5)
1	0	1	0	$w1+w3 < \theta$	(6)
1	1	0	1	$w1+w2 \geq \theta$	(7)
1	1	1	0	$w1+w2+w3 < \theta$	(8)

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From the 1st equation in the Table-15, it is transparent to us that θ must be negative, we assume $\theta = -0.5$, and$w1 = -1, w2 = 1, w3 = -1$. If these values are put into all the 8 equations in Table-15, all the equations are satisfied. Hence a solution set is $\{w_1, w_2, w_3; \theta\} = \{-1, 1, -1; -0.5\}$, with the help of this solution set we can draw its corresponding threshold logic gate which is depicted in Fig. 21.

Table-16

B	C	D	$\overline{BD+CD}$	Threshold θ	Eqn. no.
0	0	0	0	$0< \theta$	(1)
0	0	1	1	$w3\geq \theta$	(2)
0	1	0	0	$w2< \theta$	(3)
0	1	1	1	$w2+w3\geq \theta$	(4)
1	0	0	1	$w1\geq \theta$	(5)
1	0	1	1	$w1+w3\geq \theta$	(6)
1	1	0	0	$w1+w2< \theta$	(7)
1	1	1	1	$w1+w2+w3\geq \theta$	(8)

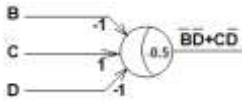

Fig.21 threshold logic gate of **e=$\bar{B}\bar{D}$+C$\bar{D}$**

Now we should be find out the threshold gate of complement of e =$\bar{B}\bar{D}$+C$\bar{D}$. For doing so, one should draw the truth table of $\bar{e} = (\bar{B}\bar{D} + C\bar{D})$and from whichwould determine the threshold logic equation.

After solving the 8 equations from the Table-16, we have obtained a solution set w1=1, w2=-1, w3= 1 ; θ=0.5. Hence taking these values a threshold logic gate of **e=$\bar{B}\bar{D}$+C$\bar{D}$** has been drawn in Fig. 22

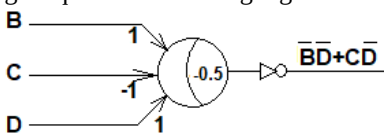

Fig.22 threshold logic gate of **e=$\bar{B}\bar{D}$+C$\bar{D}$**

Part 6: f=A+B$\bar{C}$+$\bar{C}\bar{D}$+$\bar{D}$B

Z=B$\bar{C}$+$\bar{C}\bar{D}$+$\bar{D}$B= (B+$\bar{D}$)$\bar{C}$+$\bar{D}$B……(41)

The equation (41) is linearly separable and it is determined from the space plot diagram Shown in Fig. 23 below. So we will be able to draw the linear threshold logic gate of Z =B$\bar{C}$+$\bar{C}\bar{D}$+$\bar{D}$B= (B+$\bar{D}$)$\bar{C}$+$\bar{D}$B. First we try to draw the truth table of Z and $\bar{Z}$.

Table-17

B	C	D	Z	$\bar{Z}$	Threshold θ For Z	Eqn. no.
0	0	0	1	0	$0< \theta$	(1)
0	0	1	0	1	$w3\geq \theta$	(2)
0	1	0	0	1	$w2\geq \theta$	(3)
0	1	1	0	1	$w2+w3\geq \theta$	(4)
1	0	0	1	0	$w1<\theta$	(5)
1	0	1	1	0	$w1+w3< \theta$	(6)
1	1	0	1	0	$w1+w2< \theta$	(7)
1	1	1	0	1	$w1+w2+w3\geq \theta$	(8)

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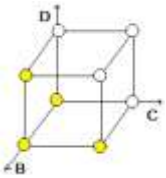

Fig. 23 space plot of Z

After being solved the 8 equations in the Table 17, a solution set is obtained as w1=-1, w2=1, w3= 1 $and\ \theta = 0.5$. So the threshold logic equation for the complement of Z=B$\bar{C}$+$\bar{C}\bar{D}$+$\bar{D}$B, i.e, $\bar{Z}$=(B$\bar{C}$+$\bar{C}\bar{D}$+$\bar{D}$B)' is given in equation(42) and the corresponding threshold logic gate is shown in Fig.24.

$Z(BCD) = sgn\{-B + C + D - 0.5\}$…… (42)

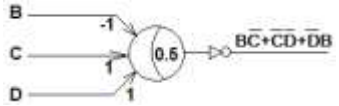

Fig. 24 TLG of Z=B$\bar{C}$+$\bar{C}\bar{D}$+$\bar{D}$B

For drawing the threshold logic gate of **f=A+B$\bar{C}$+$\bar{C}\bar{D}$+$\bar{D}$B =A+Z** which is considered as an OR gate having two variables A and Z. As we know the threshold gate of an NOR gate is $NOR(AZ) = sgn\{-A - Z + 0.5$,

So we can make the threshold logic gate of f =A+B$\bar{C}$+$\bar{C}\bar{D}$+$\bar{D}$B =A+Z, and it is drawn in Fig. 25.

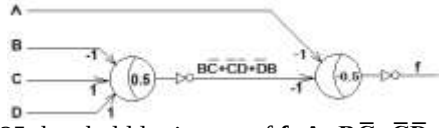

Fig.25 threshold logic gate of **f=A+B$\bar{C}$+$\bar{C}\bar{D}$+$\bar{D}$B**

Part 7: g=A+B$\bar{C}$+$\bar{B}$C+C$\bar{D}$

We divide the equation g =A+B$\bar{C}$+$\bar{B}$C+C$\bar{D}$ into two parts (i) P= B$\bar{C}$+$\bar{B}$C = B⊕C and (ii) Q=A+C$\bar{D}$. P is not linearly separable as it is an XOR Boolean logic equation that is not linearly separable. But Q is linearly separable. It is clear from space plot diagram in Fig. 26.

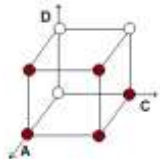

Fig. 26 space plot diagram Q=A+C$\bar{D}$

Threshold logic gate for the XOR gate is already discussed in Fig. 12(a). So our consideration part is Q=A+C$\bar{D}$. For this, we are to make the threshold logic equation. Consider the truth table of Q=A+C$\bar{D}$ given in Table-18.

After solving the 8 equations given in Table-18, we have obtained two sets of solutions $w1 = 2, w2 = 1$,

Table-18

A	**C**	**D**	**Q**	**$\bar{Q}$**	Threshold θ For A+C$\bar{D}$ 0.5	Threshold θ For **$\bar{Q}$**	Eqn. no.
0	0	0	0	1	0< θ	0≥ θ	(1)
0	0	1	0	1	w3< θ	w3≥ θ	(2)
0	1	0	1	0	w2≥ θ	w2< θ	(3)
0	1	1	0	1	w2+w3< θ	w2+w3≥ θ	(4)
1	0	0	1	0	w1≥ θ	w1<θ	(5)

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1	0	1	1	0	w1+w3≥ θ	w1+w3< θ	(6)
1	1	0	1	0	w1+w2≥ θ	w1+w2< θ	(7)
1	1	1	1	0	w1+w2+w3 ≥ θ	w1+w2+w3< θ	(8)

$w3 = -1;\ \ \theta = 0.5\}\ and\ \{w1 = -2, w2 = -1, w3 = 1\ ;\ \theta = -0.5\}$for the threshold equations of Q=A+C$\bar{D}$ and $\bar{Q}$=(A+C$\bar{D}$)' respectively**.**

The threshold equation for **Q = (A+C$\bar{D}$)**using (complement of Q plus a buffer)is given in Fig. 27 below.

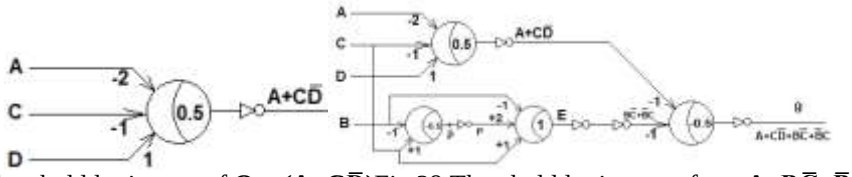

Fig. 27 threshold logic gate of **Q = (A+C$\bar{D}$)**Fig.28 Threshold logic gate of g = **A+B$\bar{C}$+$\bar{B}$C+C$\bar{D}$**

Now is our intention is to connect the two parts P and Q by using an OR gate then we will obtain g = P+Q= A+B$\bar{C}$+$\bar{B}$C+C$\bar{D}$ and the threshold gate regarding this Boolean equation is given below in Fig. 28.

Table-19

Part	*all* C_b aF	*all* C_0 aF	C_A aF	C_B aF	C_C aF	C_D aF
a	10.24, 8.5, 8.0	9.5, 9.5, 8.5	C_1^n=0.5	C_2^n=0.5	C_1^p=0.5	C_2^n=0.5
b	10.24, 8.5, 11.7	9.5, 9.5 ,8.5	--	C_1^p=0.5	C_1^n=0.5	C_2^p=0.5
c	11.7	8.0	--	C_1^n=0.5	C_1^p=0.5	C_2^n=0.5
d	9, 9.5, 10	9.5, 9, 8.5	C_1^n=0.5	C_1^p=0.5	C_2^n=0.5	C_2^p=0.5
e	9	9.5	--	C_1^p=0.5	C_1^n=0.5	C_2^p=0.5
f	9.5, 10	9, 9	C_1^n=0.5	C_2^n=0.5	C_1^p=0.5	C_2^p=0.5
g	10, 10.24, 8.5, 10	8, 9.5, 9.5, 9	C_1^n=0.5	C_2^n=0.5	C_1^p=0.5	C_2^p=0.5
All the values of input capacitances those are not cited above will be as: if input arms values are +1, -1, +2 or -2 then their corresponding will be C_x^p=0.5aF, C_x^n=0.5aF, C_x^p=1.0aF or C_x^n=1.0aF respectively, where x =1, 2. C_L =9aF, C_j = 0.25aFR_j=$10^5\Omega$, V_b =V_s=16mV. Logic "0" = 0V and logic "1"= 16mV						

All the 7-segment related threshold logic gates for the segments a, b, c, d, e, f and g are drawn above.

Now is our time to construct the threshold logic circuit/decoder for BCD to 7-segment display. And it is depicted in Fig. 29 (in separate page).

For the simulation of the BCD to 7-segment decoder shown in Fig, 29, the parameters required are givenin Table-19 and the corresponding simulation result is given in Fig.30 (in separate page). The simulation results for BCD to 7-segment converter is drawn in Fig. 30 (in separate page) by setting the simulation set on the basis of the parameters given in Table-19.

XII. DISCUSSION

We have discussed regarding 2-input AND/OR logic or 3-input AND/OR/NOR gates, XOR/ XNORand 7 segments of BCD–to-7 segment display, their corresponding circuits and simulated waveforms in due places. In addition, their threshold logic gates, by analyzing the linear separable logic equations, have been drawn. Now, the perspective analysis about their speed should be discussed. For finding out the processing delay for the cited logic gates, we should involve critical voltage $V_c$and the tunnel junction capacitanceC_j. However, considering the atmospheric temperature at T = 0K, the switching/processing delay of a logic gate can be checked with the help of the approaches [8, 9] given below.

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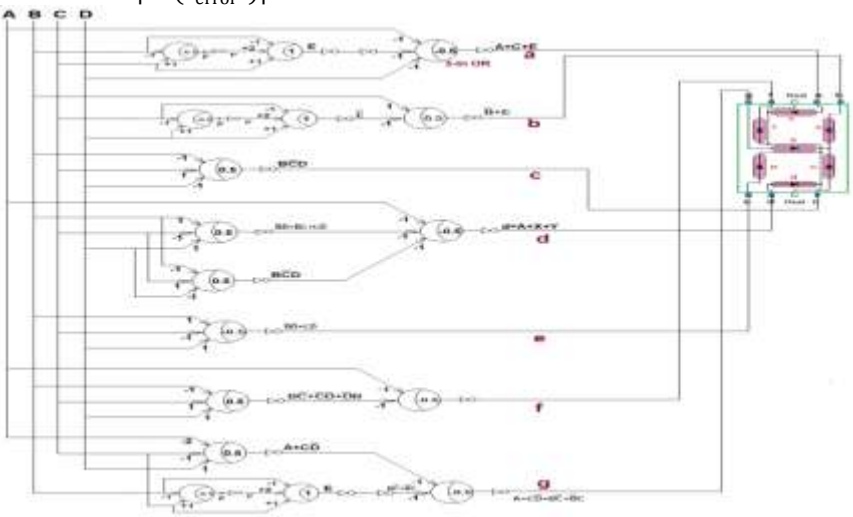
Delay = $-(e|\ln(P_{error})|R_t) / (|V_j| - V_c)$ ..... (43)
where V_j is the junction voltage and V_c is the critical voltage and $R_t$is he junction resistance.

The switching/tunnelingmust happen whenever the critical voltageV_c,of course, is less than the tunnel junction voltageV_j, i.e., $V_c < |V_j$.This happens for the case of a 2-input NOR gate in Fig-6(a)when V_{in1} is logic 1, resulting V_j =11.8mV, the critical voltage of the tunnel junction voltage V_c is 11.58mV. Considering that the probability of error change P_{error} is equal to 10^{-12} and tunnel resistsnce$R_t = 10^5\Omega$. After calculatingwe obtain a gate delay equal to $0.07281|\ln(P_{error})|$ns = 1.675 ns. In this manner, we can find out the circuit delays which are placed in Table-20. Whenever an electron goes through thetunnel junction, the amount of total energy in the circuit gets changed after the tunneling events. The difference between the energy levels before and after the tunneling event is calculated with the equation (44).

$$\Delta E = E_{before\ tunnel} - E_{after\ tunnel} = -e(V_c - |V_j|) \cdots\cdots (44)$$

This is the amount of switching/tunneling energy consumed whenever a tunnel event occurs in the tunneling circuit.



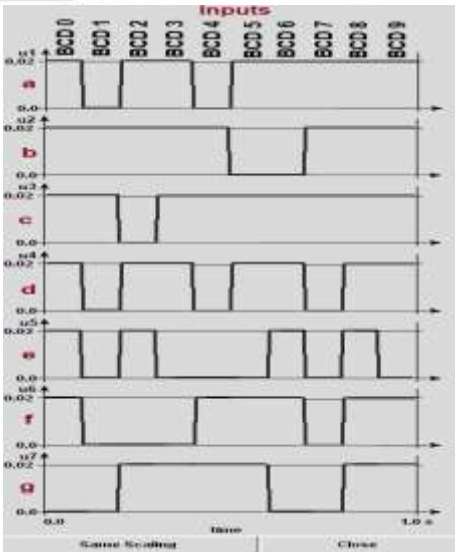


Fig.29 Threshold logic circuit of BCD to 7-segment display Fig. 30 Simulation result of BCD-to-7 Segment

We have drawn curves concerning the switching delay Vs. switching error probability in Fig. 30(a) and the switching delay Vs. the unit capacitance C shown in Fig. 30(b).

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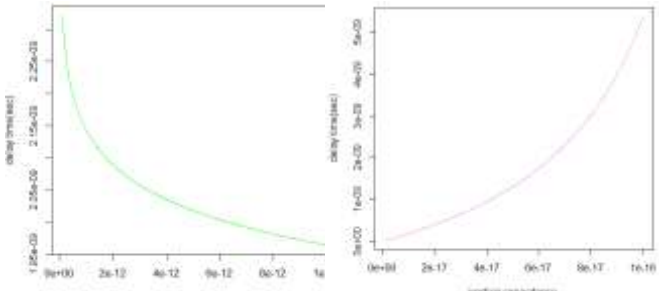

Fig. 30(a) Delay vs. Error ProbabilityFig. 30(b) Delay Vs. capacitance

We have counted the number of elementsutilizedin gates or circuits, switching delays, and switching energy consumed by the corresponding LTGs (byusing the same methodology as taken for the Boolean gates). All the calculated parameters are shown in tabular form in Table-20.

Table-20

Gate/Device	elements	Delay	Switching Energy
inverter	**09 elements**	**0.022|ln(P_{error}) | ns**	**10.4 meV**
2-input NOR	**14 elements**	**0.072|ln(P_{error})| ns**	**10.7 meV**
2-input OR	**14 elements**	**0.062|ln(P_{error})| ns**	**10.8 meV**
2-input NAND	**14 elements**	**0.080|ln(P_{error}) |ns**	**10.7 meV**
2-input AND	**14 elements**	**0.062|ln(P_{error}) |ns**	**10.8 meV**
3-input AND	**15 elements**	**0.104|ln(P_{error}) | ns**	**11.58 meV**
3-input NAND	**15 elements**	**0.072|ln(P_{error}) | ns**	**11.58 meV**
2-input XOR	**29 elements**	**0.102|ln(P_{error})| ns**	**21.2 meV**
3-input OR	**15 elements**	**0.104|ln(P_{error}) | ns**	**11.58 meV**
3-input NOR	**15 elements**	**0.104|ln(P_{error}) | ns**	**11.55 meV**
a	**44 elements**	**0.206|ln(P_{error}) | ns**	**21.1 meV**
b	**43 elements**	**0.164|ln(P_{error}) | ns**	**21.2 meV**
c	**15 elements**	**0.104|ln(P_{error})| ns**	**10.8 meV**
d	**45 elements**	**0.208|ln(P_{error})| ns**	**32.2 meV**
e	**15 elements**	**0.104|ln(P_{error})| ns**	**10.7 meV**
f	**29 elements**	**0.164|ln(P_{error})| ns**	**21.2 meV**
g	**58 elements**	**0.166|ln(P_{error})| ns**	**43.2 meV**
BCD to 7-segment	**249 elements**	**0.208|ln(P_{error})| ns**	**160.4 meV**

The element numbers and how much energy, consumed by them,are shown by vertical bars w.r.t. individual gates in Fig. 30(c).Next, we have provided the data collected from this work regarding element numbers, delays, and switching energy in Table-21.

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Table-21

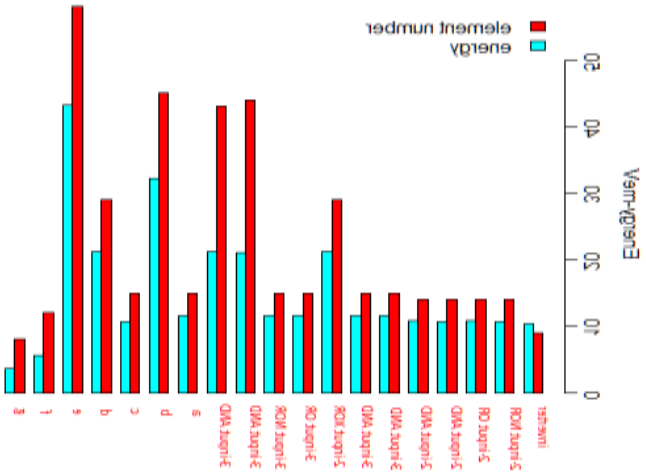

Fig. 30(c) comparison of Elements and switchingenergy of different gates

The processing delays for different threshold logic gates and circuits are different. For 2-input OR gates, the switching delay is $0.062|\ln(P_{error})|$ ns, for 3-input AND gate it becomes $0.104|\ln(P_{error})|$ ns, and for BCD-to-7-segment circuit it is $0.208|\ln(P_{error})|$ ns.

Given that the value of P_{error} equals to 10^{-12}, so the time after which the 1st output of the bit BCD-to-7-segment circuit will fan out is $0.206|\ln(P_{error})|$ ns=5.74ns. i.e., after every 5.74 ns, the next output bit will be taken from the 7-segment circuit. Therefore clock time/duration of the clock signal should be greater than or equal to 5.74 ns. In this situation, the speed of the BCD-to-7-segment circuit will be $1/5.74\text{ns} = 1.74\text{GHz}$.

We are interested in finding out the circuit delays as to CMOS, SET-based and LTG-based. The processing delay or switching delay for a CMOS logic gate like AND, NAND, NOR, XOR is 12ns [15, 16], on the other hand the time required for tunneling through a single electron transistor (SET) [9, 10] is approximately 4ns [4, 5,6, 7, 12, 13].

Switching delays of SET and LTG

It is considered that that the error probability is 10^{-12} then the delay for the 3-input OR gate will be 2.87ns and similarly the delays for the other gates can be calculated and are all shown in Table-21. It is clear to us that the LTG based circuit is faster than the SET based circuit when $P_{error} = 10^{-12}$. The comparison of delays for SET and LTG gate based circuits is represented by a bar diagram depicted in Fig.31.

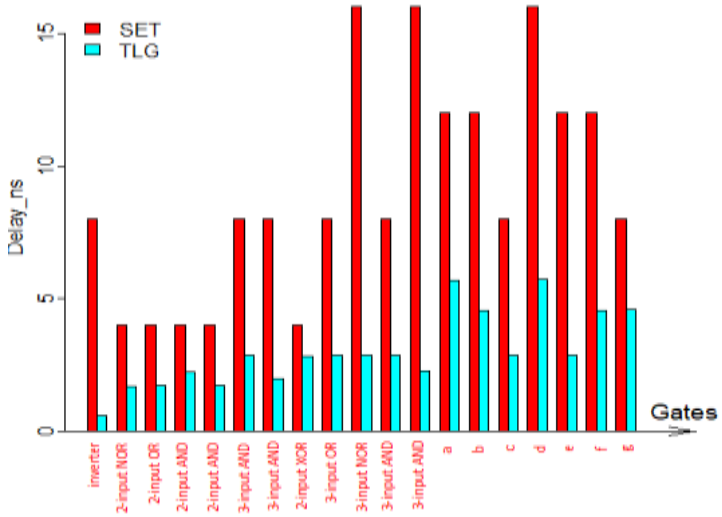

Fig. 31 Bar diagram of delays of SET/TLG Vs. gates

XIII. CONCLUSION

In this work, we have discussed the characteristic of a tunnel junction curve representing a sudden change w.r.t. input voltage i.e., tunneling event happens. Next, how and when to tunnel through for an electron is discussed. On the basis of this concept an inverter or buffer circuit is depicted and its simulation result is given. A generic Linear Threshold logic gate implementation has been discussed from which a family of logic gates is implemented. Regarding 2-inpt AND/NAND, OR/NOR, XOR, 3-input AND / NAND, OR/NOR have been enlightened with their input-output simulated results. All the threshold logic gate circuits for BCD-to-7 segment are drawn with the help of their threshold logic equations. Last, a threshold logic gate circuit for BCD-to-7 segment is depicted citing the parameters required for implementing it in tabular form and the simulated waveforms for all sections a, b, c, d, e, f and g with all possible input combinations are provided as well.All the gates or circuits requiredhave been implemented and are verified by means of simulation using SIMON. The number of elements needed for logic gates, and other circuits, their processing delays, power consumption by them are provided.It is observed that the threshold logic gates discussed are at least 2-times faster than SET based logic gates. The temperature of the operation should be kept at 0K in real situation.

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