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Design of Low voltage CMOS3.3V I/O

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ABSTRACT—Input-output (I/O) Pads are designed to interface core circuits in a system on chip to external world. Different types of Input-Output (I/O) are available for different applications, such as Low voltage differential signaling (LVDS) based general purpose input output (GPIO), and Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) based GPIO. Most of the low power embedded applications require GPIOs operating at normal frequency range. For this LVCMOS 3.3 based I/O design is more appropriate to meet the power and area constraints. The bi-directional Low voltage complimentary MOS (LVCMOS33) is designed for the specification given to us and simulated in Cadence virtuoso 6.1.5 using UMC (United Microelectronics Corporation) 180 nm technology and verified across all the process corners, voltage and temperature variations.
Keywords—I/O,LVDS, GPIO, LVCMOS, MOS, UMC

I. INTRODUCTION

Input-Output (I/O) Pads are designed to interface core circuits in system on chip to external world. The signal which is propagating all along in silicon has to come out of the chip and delivered to external world through package. This I/O package is a circuit, which sits at the interface of the chip, and transfers the signal from and to chip core (silicon) and external world [1].

INTRODUCTION INPUT-OUTPUT

Types of I/O

1. Input (uni-directional) 2. Output (uni-directional) 3. Bi-directional 4. Open-drain5. Low Voltage Differential Signalling (LVDS)

Detailed explanation is given below

1. Input : The input buffer passes external data to the core. It performs the level conversion from the external voltage to the core voltage level. It helps improve the signal by performing signal conditioning

2.Output (2-state or 3-state) : The output buffer passes data from the core to the external world which is usually another component on the Printed Circuit Board (PCB) through a track. It performs level conversion from the core level voltage to the IO level output voltage (the motherboard voltage level).

3. Bi-directional : A bi-directional buffer functions as both an input and an output buffer.

4. Open-drain : Open-drain buffers come with pull-up resistors instead of a PMOS transistor. This pull up resistor is external to the chip mostly and needs to be connected to the specified termination voltage (VTT).

5. Low Voltage Differential Signalling (LVDS) : Differential buffers can also be used depending on the application. LVDS buffers help achieve higher speed, lower power dissipation, and common-mode noise rejection compared to a single-ended buffer. But, these advantages come at the design cost of time and money.

We are using bi-directional Input-Output system for our design. The block diagram of the same is given below in Figure 1.2. A Bi-directional Input-Output (I/O) system consists of : 1. Transmitter (Driver) 2. Receiver 3. Pull-up / Pull-down logic 4. ESD protection circuitry.

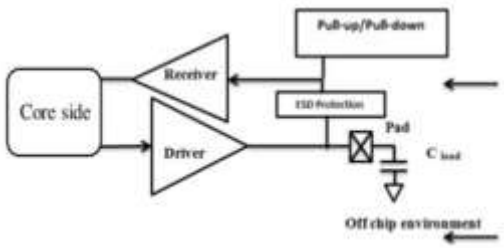

Figure 1.2:Bi directional IO block

TRANSMITTER

The output pad that is LVCMOS transmitter is used to transmit the signal from core to outside world. From the block diagram of GPIO as shown in the Figure 1.3, the LVCMOS transmitter block diagram is characterized and implemented in this project. The module of LVCMOS based transmitter consists of three modules. They are level shifter, pre driver and driver. The transmitter is used to transmit the signal from core to the outside world, since core operates at low voltage levels. It has to be level up shifted to higher voltage levels, since pad operates at high voltage levels. To convert core voltage to pad

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voltage we use level up shifters (Contention Mitigated Level Shifter) and pass the signal to control logic and pre driver stage in which pre driver is used to drive the huge driver and the control logic is used to control the operation of the transmitter. The detail analysis is discussed in the further chapters.

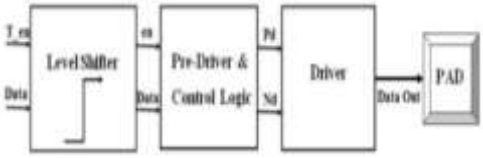

Figure 1.3: Transmitter block diagram

1. Level up shifter The name Level up shifter itself states that its used to translate voltage domains i.e translation from one voltage domain to another voltage domain.
2. Driver Circuit design is performed according to the target specification provided, using the Cadence tool environment. It has pre-drive and driver circuit. Pre-driver is used drive the load of level up shifter. The drive should be able to pull atleast 16 mA in worst case PVT analysis. Then a chain of driver is added after pre-driver to be able to drive the external load.
3. ESD ESD stands for electro static discharge. ESD is the major problem which results in IC failure. About 35 percentage of the total IC failure is cause by ESD. It is basically a charge balancing act that happens when we touch the IC surface. It cab happen through direct contact or through induces external electric field. There are many models which represents the ESD model they are: (a) Human body model (b) Machine Model (c) Charged device model .

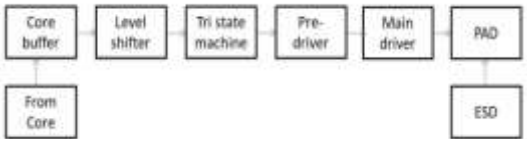

Figure 1.4: Transmitter block

Receiver:

Receiver, pullup and pulldown circuit are being designed and implemented . The receiver block diagram is shown in Figure 1.5. It consist of Schmitt Trigger, Level down shifter for controlling of the signals. The working of receiver is as follows: The received signals from the external circuit are passed through the Schmitt Trigger to remove noise present. Since the core is operating at 1.8 V and I/O is operating at 3.3 V the received signals are to be level shifted to 1.8 V using level down shifter. The detailed explanation of each block is explained in following sections.

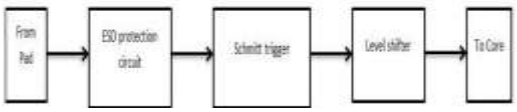

Figure 1.5: Receiver block

1. Schmitt Trigger Schmitt triggers are bistable networks used widely to reduce the noise and disturbance of the circuit. The output of the Schmitt trigger varies from low to high for the falling edge of the curve and the curve changes from high to low for the rising edge of the curve. When the input of the Schmitt Trigger is exceeding VOH, the output switches to low, and the input should go below VOL to get the output as low The Schmitt Trigger works as the normal inverter when both VOH=VOL. Hysteresis of the Schmitt Trigger is given by VHY S= VOH-VOL.
2. Level-down shifter A level-down shifter is used to translate signals from higher voltage domain (3.3 V) to lower voltage domain (1.8 V),to allow the compatibility between the stages of the IC (Integrated Circuit).

[2]Design and Implementation

Transmitter: It consists of two blocks : Level Up Shifter, Driver and Pre-Driver. It transmits the signal from core to external world. Level up Shifter The Figure 2.1 is the schematic of the Level-up shifter. The circuit is also called as Contention Mitigated Level Shifter. Input is given at Vin as shown in Figure 2.1. Output is taken across the capacitor of 100 pf.

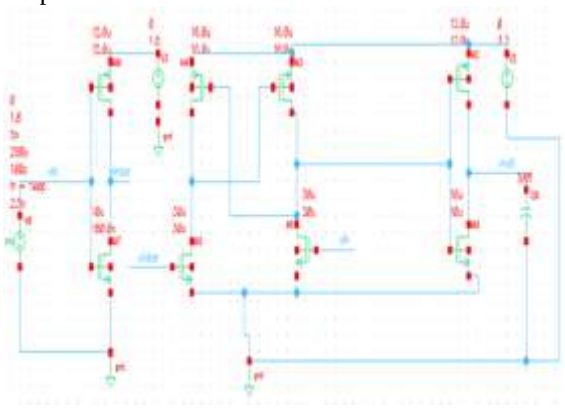

Figure 2.1: Level up shifter circuit diagram

The design is done by calculation the beta ratio of the second stage of the level shifter. An input pulse varying from 0 V to 1.8 V having a frequency of 200 MHz is given to Vin. The below Figure 2.2 is the symbol of levelshifter In =0.5*kn' *(Wn/L)*(Vgs-Vtn),Ip=0.5*kp'*(Wn/L)*(Vsg-Vtp),In/Ip=0.5 *kn'*(Wn/L)*(Vgs-Vtn) /0.5*kp'*(Wn/L)*(Vsg-Vtp).

International Journal of Advances in Engineering and Management (IJAEM)
Volume 3, Issue 9 Sep 2021, pp: 960-966 www.ijaem.net ISSN: 2395-5252

Assume Vtp=Vtn=0.5 V and length of MOSFETs are same.
Vgs=0.9 ,Vsg=1.65V (Both MOSFETs are in saturation) .In/Ip =0.5*kn'*(Wn/L)*(0.9-Vtn) /0.5*kp'*(Wn/L)*(1.65-Vtp) Wp /Wn =0.1209,We know Un/Up=3,Therefore Wn= 2.755*Wp.

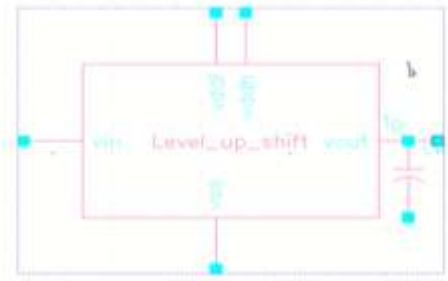

Figure 2.2: Symbol

Driver:

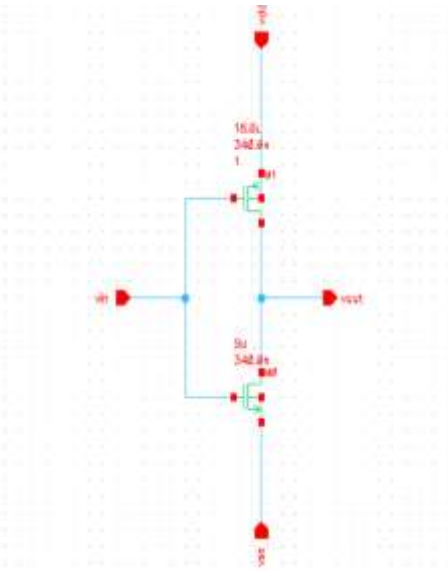

Figure 2.3: Circuit Diagram

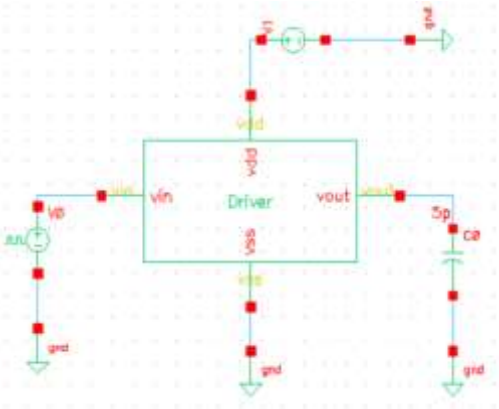

Figure 2.4: Symbol

The width (size) of the P-driver is designed by connecting VOH at the PAD and varying the width until the driver is able to source -2 mA of current at the worst operating condition. (VDD-VOH)/ RON =-2mA. Ron =1/ Bp(VDDIO- —VTp —). Bp = Mp.Cox(W / L) p. Where :Mp=mobility of holes. Cox=the capacitance of the gate oxide of the PMOS transistor.

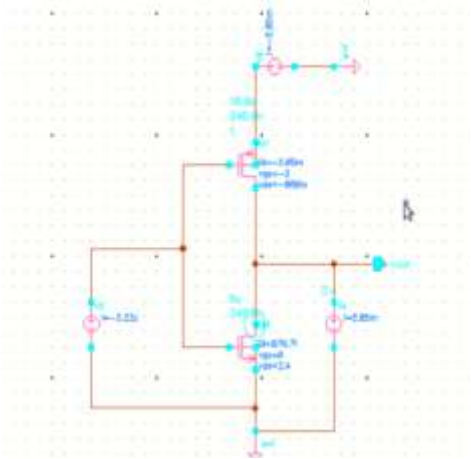

Figure 2.5: P-driver design

Receiver: Consists of circuit diagram of Schmitt trigger and level down shifter.Its a circuit diagram of Schmitt trigger without a output buffer.

International Journal of Advances in Engineering and Management (IJAEM)
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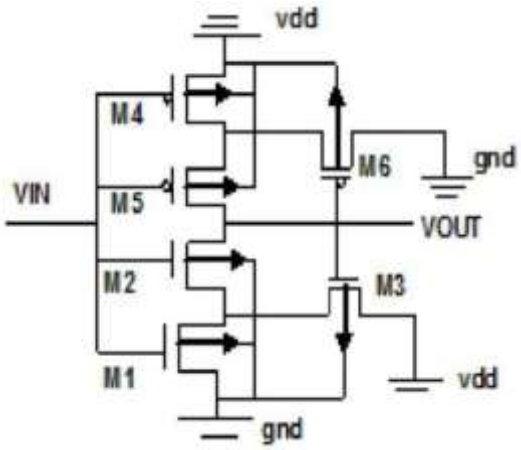

Figure 2.6: Circuit Diagramof Schmitttrigger

Schematic of Schmitt trigger with output buffer [3]. The output buffer helps to remove unwanted spikes and makes the output wave crisper.

Figure 2.7: Schematic of Schmitt trigger

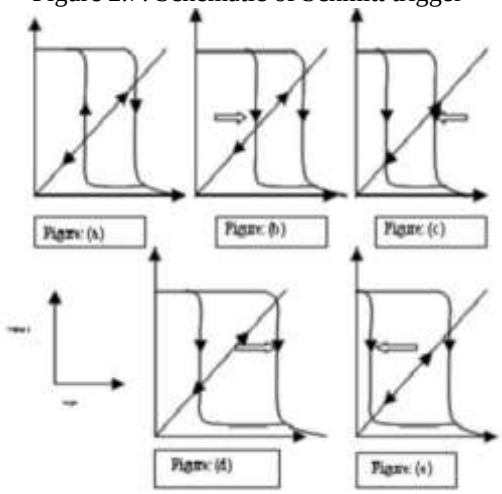

Figure 2.8: Schematic of Schmitt trigger

(a) General Case (when width of any MOSFETs are not changed), (b) As width of MOSFET 'M4' of Fig 2.6 Increases, (c) As width of MOSFET 'M1' of Fig 2.6 Increase, (d) As width of MOSFET 'M3' of Fig 2.6 Increase, (e) As width of MOSFET 'M6' of Fig 2.6 Increase.

Symbol:It has four pins i.e vin, vout, vdd, gnd.

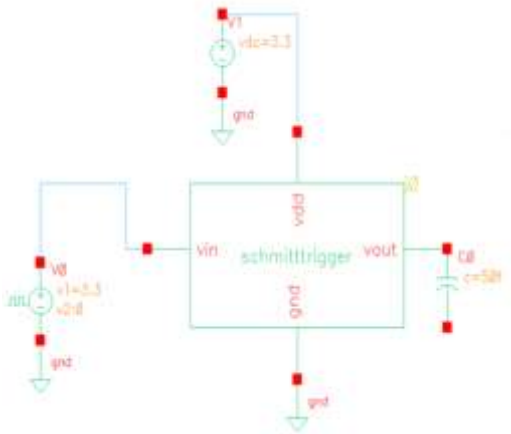

Figure 2.9: Symbol of Schmitt trigger

Level down shifter:It shifts the voltage from 3.3 to 1.8 V. Level down shifter is used for converting the voltage.levels from 3.3 V to 1.8 V . Since the pad operates at 3.3 V and core operates at 1.8 V we require a level down shifter to convert the signals coming from Schmitt trigger to core voltage signals.The figure 2.9 shows the circuit of level down shifter. It consists of a simple inverter and a cross coupled network.

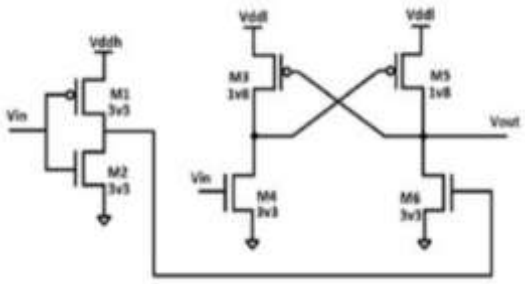

Figure 2.10: Circuit Diagram of Level down shifter

[3]Results:

This chapter gives detailed explanation of output result and anlysis of across all the corners like tt, ss, ff, snfp, fnsp [2].

Transmitter:in Level up shifter,The figure 3.1 shows the voltage translation from core voltage(1.8v) to external world voltage(3.3V).

International Journal of Advances in Engineering and Management (IJAEM)
Volume 3, Issue 9 Sep 2021, pp: 960-966 www.ijaem.net ISSN: 2395-5252

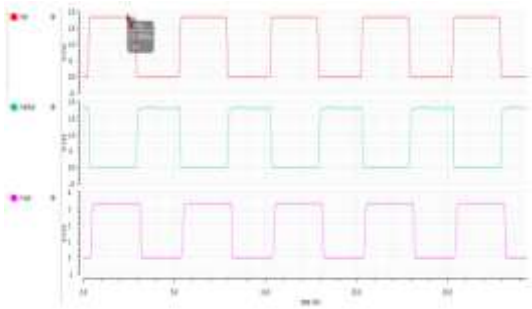

Figure 3.1: Output of level up shifter(1.8V to 3.3V)

Corners	tr(27)	tf(27)	tr(-40)	tf(-40)	tr(125)	tf(125)
tt	90.56ps	55.82ps	80.53ps	43.181ps	102.819ps	79.18ps
ss	96.242ps	52.731ps	103.684ps	65.501ps	123.15ps	82.192ps
ff	83.11ps	53.29ps	76.45ps	43.281ps	95.52ps	64.285ps
snfp	95.423ps	56.3126ps	84.558ps	45.859ps	112.848ps	73.725ps
fnsp	93.026ps	55.359ps	86.961ps	46.87ps	16.89ps	75.937ps

Figure3.2: Characterization of level shifter across pvt [1.8v,3.3v]

Corners	-40 Degree celsius	27 Degree celsius	125 Degree celsius
tt	1.68	1.73	2.12
ss	1.92	2.2	2.402
ff	1.52	1.89	2.23
snfp	1.57	1.62	1.89
fnsp	1.82	2.3	2.48

Figure 3.3: DCD values (in percentage) [1.8v,3.3v]

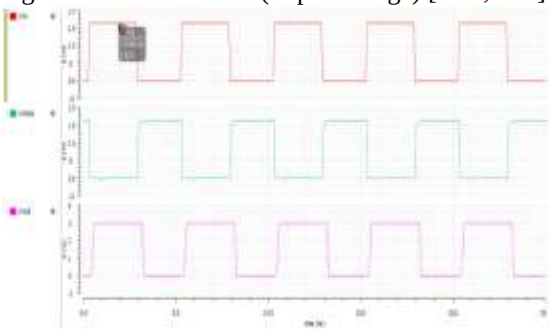

Figure 3.4: Outputs of level up shifter considering the worst case analysis (1.62V to 2.97V)

Corners	tr(27)	tf(27)	tr(-40)	tf(-40)	tr(125)	tf(125)
tt	198ps	103ps	155ps	91ps	225ps	135ps
ss	229ps	115ps	184ps	97ps	260ps	147ps
ff	96ps	166.28ps	154.4ps	82.3ps	195.3ps	109ps
snfp	180.5ps	105.4ps	153.2ps	91.49ps	215.5ps	126.3ps
fnsp	197.3ps	100.5ps	168.4ps	88.3ps	234.5ps	120ps

Figure 3.5: Characterization of level shifter across pvt[1.98v,3.63v]

Corners	-40 Degree celsius	27 Degree celsius	125 Degree celsius
tt	0.48	0.76	1.08
ss	0.16	0.56	1.08
ff	0.67	0.84	1.08
snfp	0.48	0.03	0.48
fnsp	0.99	1.18	0.92

Figure 3.6: DCD values (in percentage)[1.98v,3.63v]

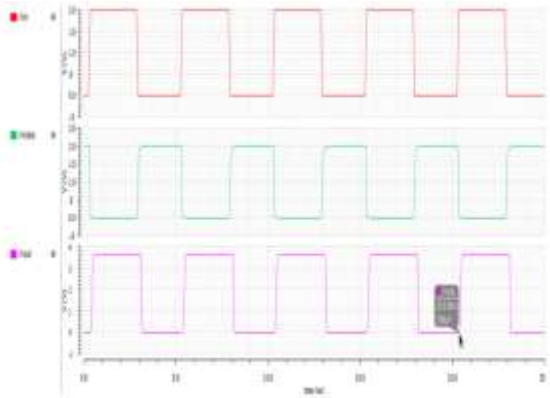

Figure 3.7: Output of level up shifter considering the worst cases(1.98,3.63)

Corners	tr(27)	tf(27)	tr(-40)	tf(-40)	tr(125)	tf(125)
tt	161ps	99ps	148ps	88.5ps	186.5ps	110.2ps
ss	180ps	102.78ps	165ps	89.2ps	215ps	129s
ff	152.2ps	87ps	129ps	78.25ps	165ps	111ps
snfp	155.3ps	99.22ps	132.5ps	85.3ps	188ps	116.7ps
fnsp	177ps	91.9ps	155.5ps	82.34ps	197.58ps	116.8ps

Figure 3.8: Characterization of level shifter across pvt[1.98v,3.63v]

Driver:

a)TT corner

Temperature(in Celsius)	-40	27	25
P Driver Current	-2.411 mA	-2.01 mA	-1.72 mA
N Driver current	2.319 mA	2.017 mA	1.65 mA

Figure 3.9: Analysis across PVT

b)SS corner:

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Temperature (In Celsius)	-40	27	125
P Driver current	-2.108mA	-1.772mA	-1.465mA
N Driver current	2.36mA	2.043mA	1.685mA

Figure 3.10: Analysis across PVT

c)FF corner:

Temperature(in Celsius)	-40	27	125
P Driver current	-2.701mA	-2.324mA	-1.982mA
N Driver current	2.675mA	2.376mA	2.013mA

Figure 3.11: Analysis across PVT

Receiver:a)Schmitt trigger

DC analysis where VIH = 0.7 * VDDO= 2.31 V VIL = 0.3 * VDDO= 0.99 V Vhys = 0.4 * VDDO= 1.32 .

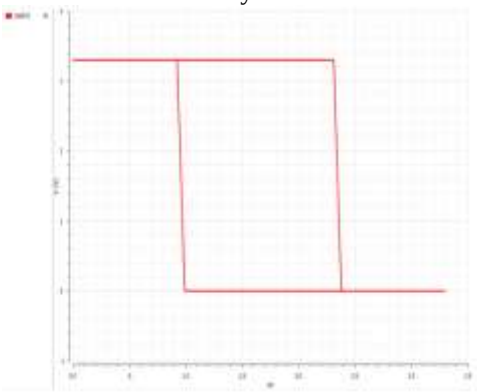

Figure 3.12: DC analysis hysteresis curve

The top waveform is the output taken across the capacitor. The bottom waveform is the input given.

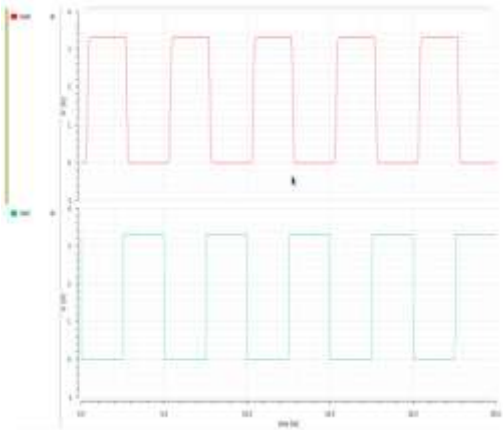

Figure 3.13: Transient analysis output

	Expected		Simulated		Process Corner	
	Min	Max	Min	Max	Min	Max
Rise_time (ps)	0	500ps	85.76ps	116.4ps	FF	SS
Fall time (ps)	0	500ps	46.9ps	65.6ps	TT	SS
T_r-T_f (ps)	0	500ps	38.13ps	66.3ps	FF	TT
Delay	0	500ps	55.6ps	75.2ps	FF	SS
DCD	0	250ps	25.6ps	55.1ps	TT	SS
V_{oh}	2.97V	3.63V	1.26V	1.29V	TT	SS
V_{ol}	0.891	1.089	0.53V	0.541V	TT	SS

Figure 3.14: Analysis across PVT

b)Level down shifter

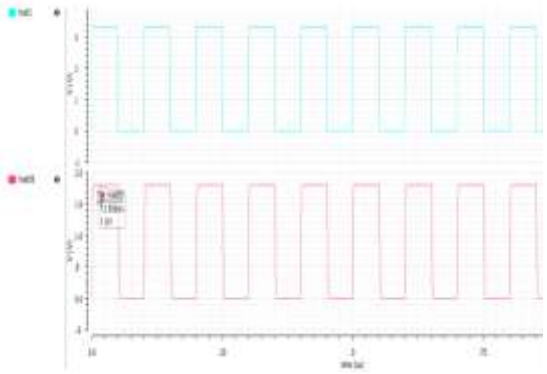

Figure 3.15: Transient analysis

[4]Physical design

Introduction to physical design: The next part of the project involves the layout of the LVCMOS I/O Pad using the cadence virtuoso layout tool. The Individual blocks are designed. The layout of all sub-blocks are shown in following figures respectively.

a)Level up shifter layout

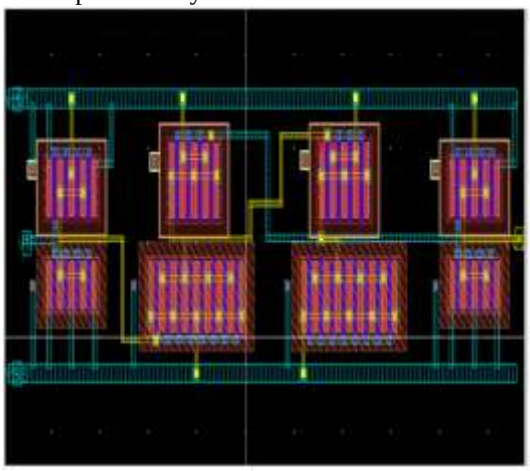

Figure 4.1: Layout Level up shifter

International Journal of Advances in Engineering and Management (IJAEM)
Volume 3, Issue 9 Sep 2021, pp: 960-966 www.ijaem.net ISSN: 2395-5252

b)Schmitt trigger layout

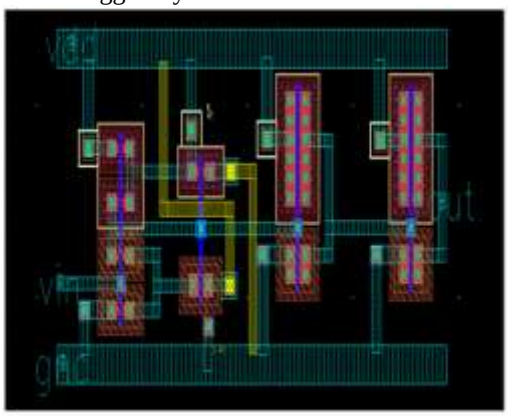

Figure 4.2: Layout Schmitt trigger

c) Driver and pre-driver

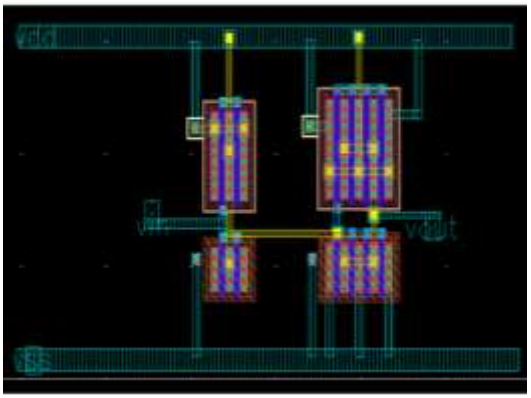

Figure 4.3: Layout Schmitt trigger

Some of the things which are given emphasis while laying out the circuit are: 1. Substrate contacts are provided so that chances of latch-up are reduced. 2. Metal-1, Metal-2 are used for signal routing. 3. Care is taken to make the power plan as robust as possible by having wider metals and maximum number of vias. 4. The layout has no LVS (Layout Versus Schematic) and DRC (Design Rule Check) errors.

II. CONCLUSION AND FUTURE SCOPE:

We have designed a level shifter, driver, Schmitt trigger, ESD protection circuit according to given specifications and we have verified the results across each corner and at different temperatures and our results matched with the given specifications. Using these designs, we can develop LVCM -OS33 receiver and transmitter IO design for different specifications. We can increase the compactness of the IC's, for different frequencies.

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