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Design of 6T-SRAM Cell Using SKY130 PDK

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ABSTRACT- The paper describes design, analysis and implementation of SRAM IP (6T-cell) using Skywater SKY130 PDK technology. It is implemented using 130nm CMOS technology node to work on operating voltage of 1.8V with access time less than 2.5ns.
Keywords— SRAM, 6T-cell,Skywater, SKY130

I. INTRODUCTION

With the advent of technologies like IoT and low power embedded applications, need for low power, fast access memory has grown substantially. SRAM with high speed, high performance and reliability fits into the demand. With the rise of open-source tools, it is now possible to design, implement and fabricate a memory IP using open-source based design flow. This paper explores this possibility with use of SKY130 PDK and other open-source tools.

II. ARCHITECTURE AND WORKING

A. Architecture of SRAM

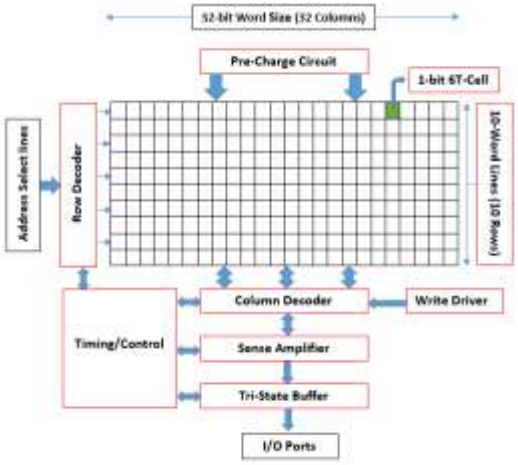

Fig. 1 SRAM Architecture

The above fig. shows the architecture of SRAM. The decoders are used for selecting a particular cell/memory bit. A sense amplifier is used as a peripheral to the memory array to sense differential voltage/current on the bit line in read operations to give amplified output to I/O ports [1]. The pre-charge circuitry is present to keep bit lines high.

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B. 1-bit 6T-cell

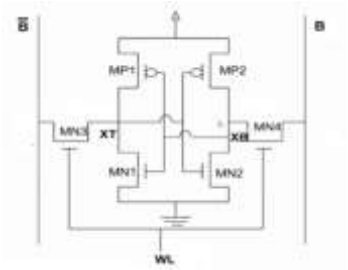

Fig.2 6T SRAM Structure

Every cell is made up of 2 crossly coupled CMOS inverters and 2 pass/access transistors (NM3, NM4) to read and write data. Refer Fig. 2.

Read Operation: Assume XB ='1' and WL ='1' which enables NM3 and NM4 and thus the values of XB and XT are transferred to bit lines by keeping B high and discharging ~B through NM3, NM1 [2].

Write Operation: Assume B='1' and WL='1', then XB='1' discharges through bit line and becomes '0'. The XT can't become '1' due to read stability and the new value of XT is set by NM4 which is connected to XT inverter [2].

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III. IMPLEMENTATION

A. 6T Cell

A simple 6T cell has been designed using the basic MOSFETs available in the PDK.

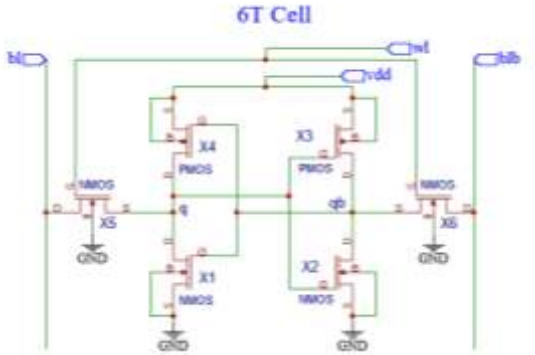

Fig. 3 6T Cell

B. Sense Amplifier

A simple sense amplifier design is shown in Fig 4. This is used to sense the voltages on the bit-lines of the cell and give output as per the read/write operation.

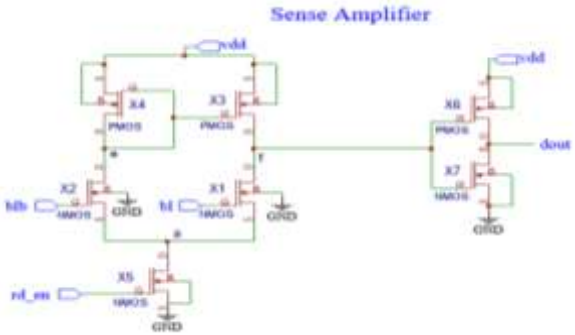

Fig. 4 Sense Amplifier

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C. D Flip Flop

A D-FF is an essential element in the SRAM circuitry for read/write operation [3]. The design for a positive edge D-FF is shown in Fig. 5.

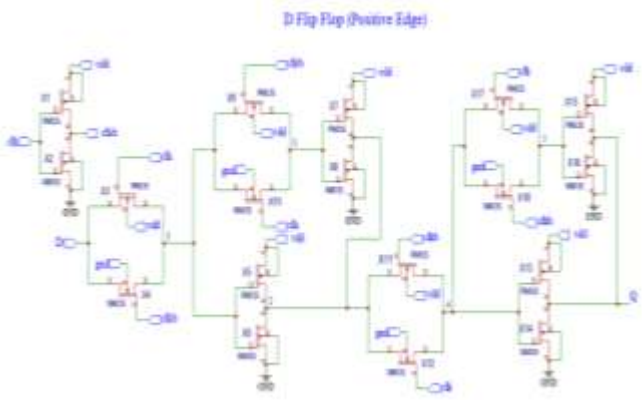

Fig. 5 D Flip Flop

D. Tristate Buffer

A Tristate Buffer is an essential element in the SRAM circuitry for read/write operation [4]. The design for a positive edge D-FF is shown in Fig. 6.

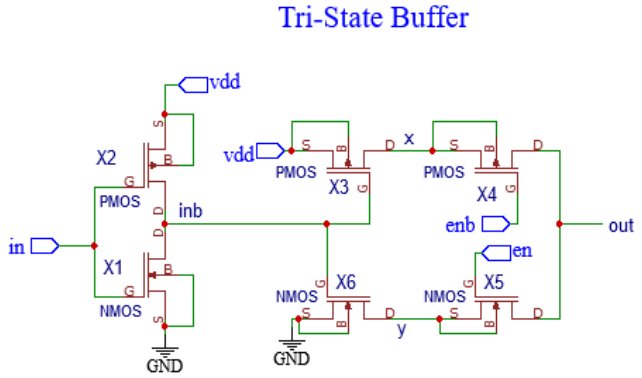

Fig.6 Tristate Buffer

E. Write Driver Circuit

Fig 7. Shows the write driver circuitry. This circuit discharges a bit line from a pre-defined pre-charge level to the write margin level. A pre-charge circuitry is also shown in the figure [5].

Fig. 7 Write Driver Circuit

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IV. RESULTS AND ANALYSIS

A. 6T Cell Read

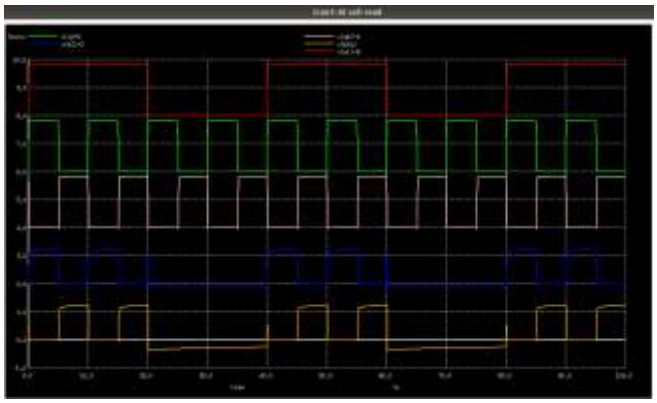

Fig. 8 6T Cell Read

Fig. 8 shows that whenever WL is low, there is no read operation and whenever WL is high, the data is being read correctly.

B. 6T Cell Write

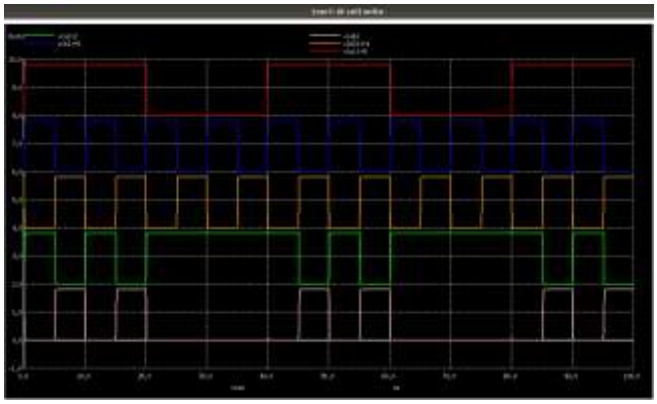

Fig. 9 6T Cell Write

Fig. 9 shows write shows that whenever WL is high, the data is being written properly as shown by q and qb.

C. 6T Cell Stability

a) SNM Calculations:

The stability and writability of the cell are quantified by the hold margin, read margin and write margin which are determined by the static noise margin (SNM). It determines how much noise can be applied at the inputs of the two cross coupled inverters before a stable state is lost during hold or read operaring mode or a second stable state is created during write operation.

b) Hold SNM

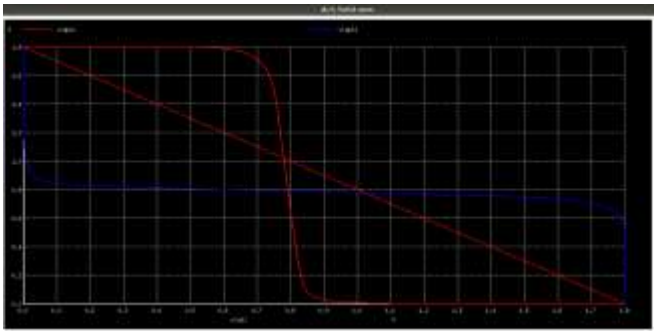

Fig. 10 Hold SNM

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By fitting a square in the upper and lower loop, we get SNMh = 0.78V and SNMl = 0.67V respectively. Hold SNM = min (SNMh, SNMl) = 0.67V

c) Read SNM

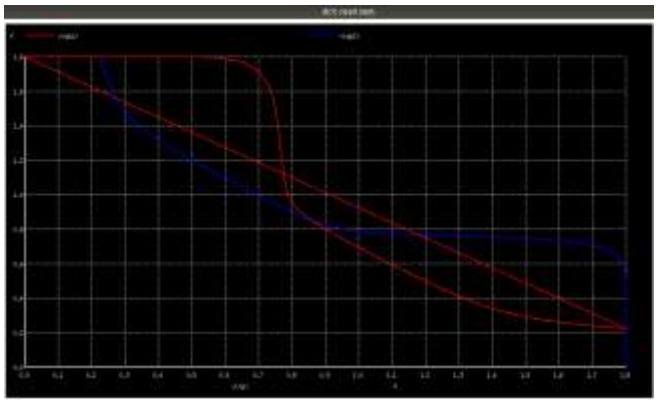

Fig. 11 Read SNM

Similarly
Read SNM = min (SNMh, SNMl) = 0.38V

d) Write SNM

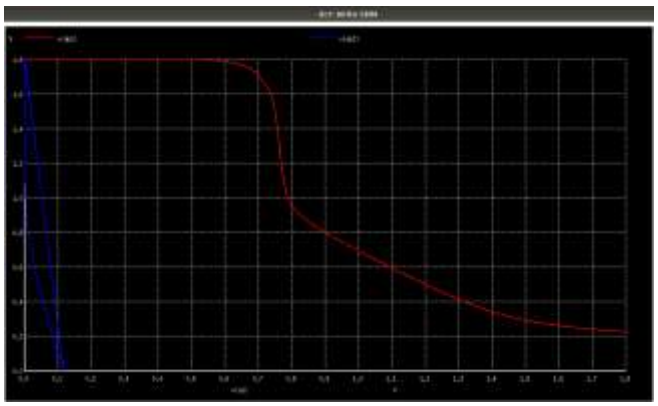

Fig. 12 Write SNM

By fitting the smallest square between the two curves, we get
Write SNM = 0.79V

e) N-Curve

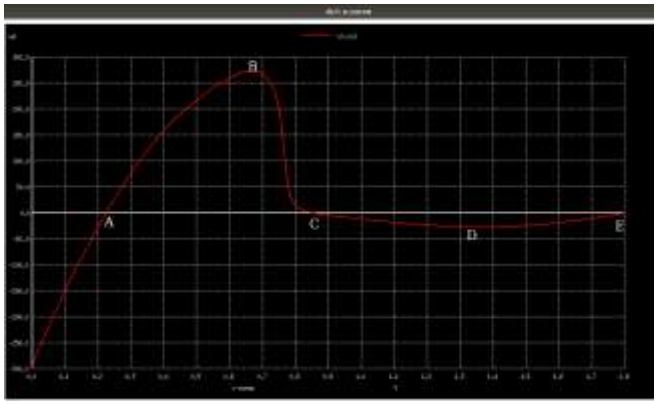

Fig. 13 N-Curve

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Read Stability Metrics

Static Voltage Noise Margin (SVNM) - It is the maximum tolerable dc noise voltage at internal nodes of the bitcell before its content flips and it is measured as the difference between point C and point A.

SVNM = 0.630 V

Static Current Noise Margin (SINM) - It is the maximum tolerable dc noise current injected at internal nodes of the bitcell before its content changes and it is denoted by point B.

SINM = 272.92 uA

Write Stability Metrics

Write Trip Voltage (WTV) - It is the minimum voltage drop needed to change the internal nodes of the bitcell and it is measured as the difference between point E and point C.

WTV = 0.946 V

Write Trip Current (WTI) - It is the minimum amount of current needed to write the bitcell and it denoted by point D.

WTI = -29.17 uA

D. Sense Amplifier

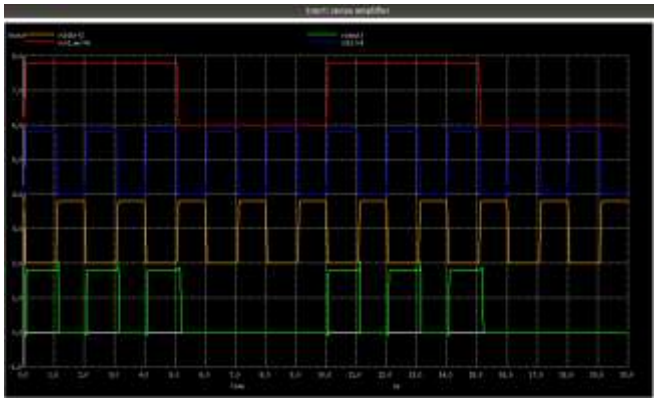

Fig. 14 Sense Amplifier

Here we can see that whenever read enable is high, the sense amplifier output is reading the data and giving us the proper output.

E. Write Driver

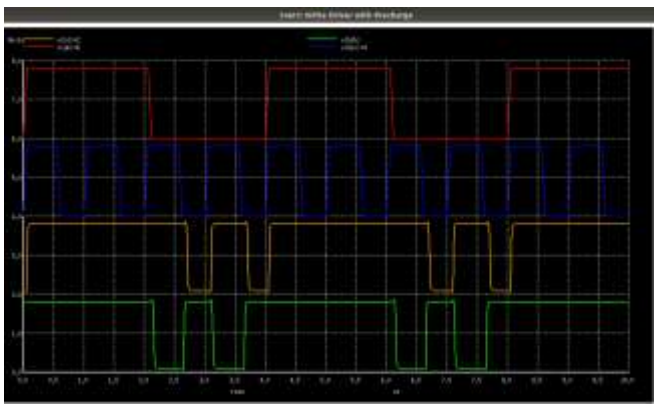

Fig. 15 Write Driver

Here we can see that the write driver circuitry is working properly and writing the required data into the cell.

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F. Tristate Buffer

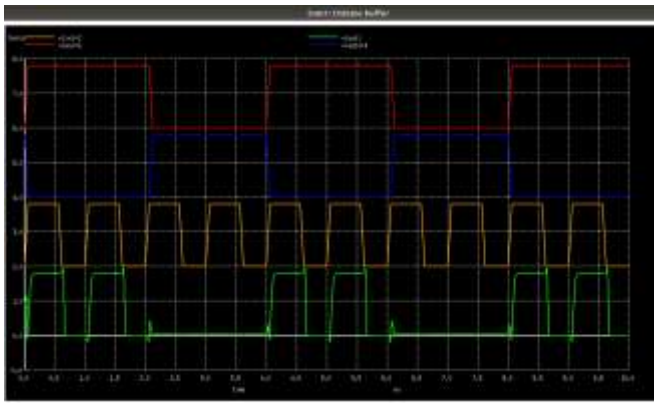

Fig. 16 Tristate Buffer

Here we see that the tri-state buffer is working properly.

G. Positive Edge Trigged D Flip Flop

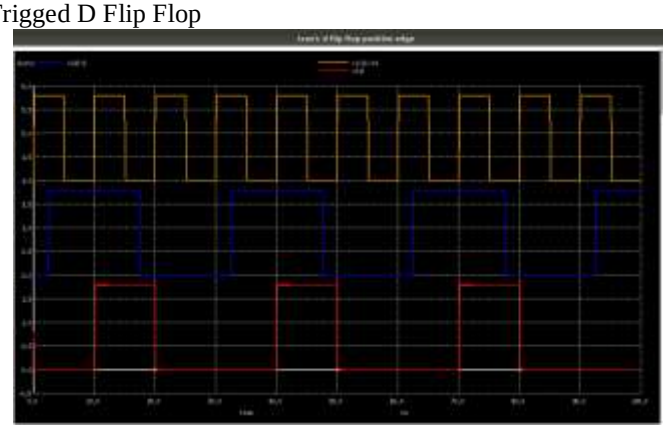

Fig. 17 D Flip Flop

Functionality of D-FF is verified through this simulation result.

H. 1-bit SRAM Architecture

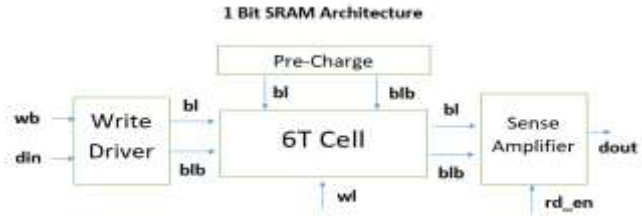

Fig. 18 1-bit SRAM Architecture

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I. Read Operation

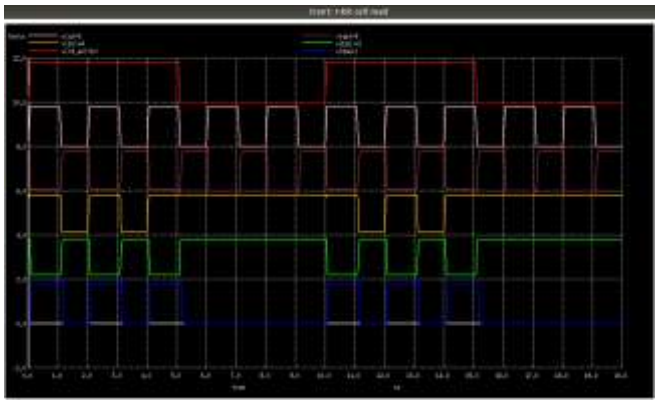

Fig.19 Read Operation

J. Write Operation

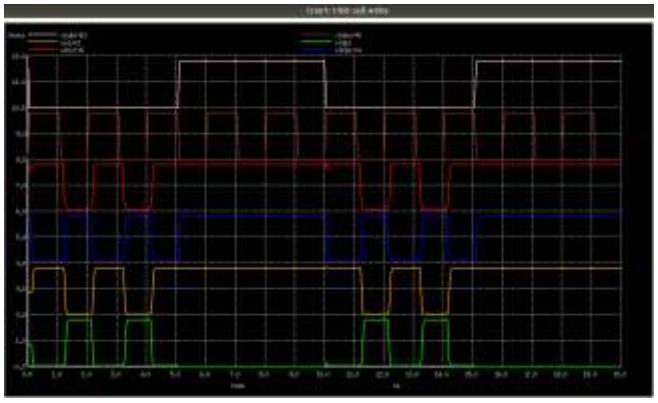

Fig. 20 Write Operation

This verifies the write operation on 6T cell with all auxiliary circuitry.

V. CONCLUSION

Thus, a simple 6T SRAM cell was designed using open source PDK (SKY130) and other open source tools. Its functionality was verified through spice simulation.

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