International Journal of Advances in Engineering and Management (IJAEM)
Volume 2, Issue 1, pp: 841-846 www.ijaem.net ISSN: 2395-5252

Design and Analysis of Low Power and High Speed Double- Tail Comparator Using Power Gating Techniques

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Date of Submission: 22-06-2020 Date of Acceptance: 10-07-2020

Abstract: Comparator is a device that compares two inputs and gives a binary output. It plays a vital role in Data converters, Signal processing system and sensing circuits. It is the basic building block of Analog-to-Digital Converters (ADCs) as they require comparators of low power consumption and high speed.In this paper, we have proposed the design of Double-Tail comparators using power gating techniques as it increases the switching speed and also the comparison of power dissipation and delay between the Conventional, Coarse grain and Fine grain double-tail comparators is presented. The designed Double-Tail comparators is simulated using Mentor graphics tool with 130nm CMOS technology. From the simulation result it is observed that the power dissipation and delay are reduced and we can observe the minimal value in Fine grain double-tail comparator.

Keywords: Analog-to-Digital Comparators(ADC),Double-Tail comparators, Switching speed, Conventional Double-Tail comparator, Coarse grain Double-Tail comparator, Fine grain Double-Tail comparator, Mentor graphics, CMOS technology.

I. INTRODUCTION

During the present days the demand for portablebattery operated devices is increasing, and the main importance is given to low power methodologies for high speed applications. As we have to minimize the power consumption by using smaller feature

size processes. The comparators are also called as 1-bit Analog-to-Digital Converters. comparators that are used in ADCs requires less power dissipation, high speed, less delay, less offset voltage, low noise, better slew rate, less hysteresis etc for achieving these the comparator should be tightly constrained. The dynamic comparator is used in ADCs now-a-days as they are having high speed, less power dissipation, zero static power consumption. The back-to-back inverters in dynamic comparator provide positive feedback mechanism which converts the small voltage difference into full scale digital level output.

Comparator is the circuit which gives the binary output by comparing two voltages or currents. These are basically used in the Analog-to-Digital Converters(ADCs) and during this conversion process, the analog input signal is first sampled and that is applied to the comparator to get the digital value for the input analog value. The logical value given by the comparator says whether the input is higher or lower than the other input. Here the inputs that are compared are analog voltage and reference voltage. The output of the comparator can either be Logic '1' or Logic '0'.

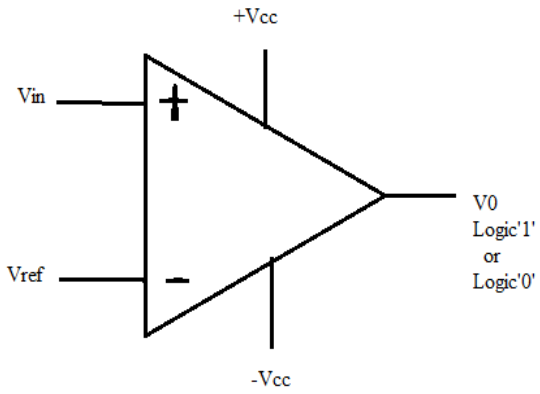

Figure 1: Basic Comparator

The output of the comparator can be logic '1', if the analog voltage is greater than the reference voltage and the output can also be logic '0', if the analog voltage is lesser than the reference voltage.

If Vo = Logic '0' then Vin <Vref
= Logic '1' then Vin >Vref

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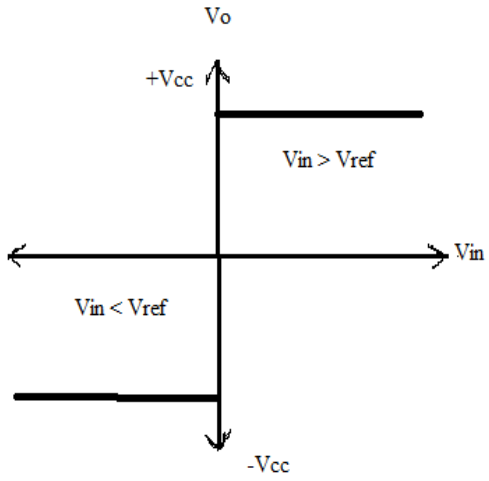

Figure 2: Transfer characteristics of comparator

The comparator consists of mainly three blocks they are pre-amplifier, latch comparator and output buffer.

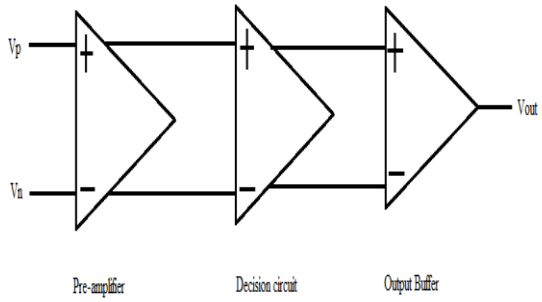

Figure 3: Comparator Architecture

The preamplifier based latched comparators are their high speed and low input referred latch offset voltage. The basic principle behind the preamplifier based comparator is to use a preamplifier to build up the input change to a sufficiently large value and then apply it to the latch. The preamplifier stage amplifies the input signal to improve the comparator sensitivityand isolate the input of the comparator from the switching noise coming from the positive feedback stage. The decision circuit is used to determine which of the input signals is larger and extremely amplifies their difference. The output buffer amplifies the information from latch and gives digital signal as output.

In order to reduce power consumption in comparators power gating technique is proposed. In this technique, the circuit operates in sleep mode by switching off the current in the circuit which is not used for a short a period by doing this the power dissipation is reduced. The platform used to design and analyze the circuits is Mentor graphics tool.

The research paper is organized as follows: an introduction to the comparator followed by each comparator circuit operation and its architecture. Finally, the simulation result for all the architectures are shown and discussed.

II. CLOCKED REGENERATIVE COMPARATOR

The dynamic and double-tail comparators are clockedregenerative comparators which are used in many high –speed ADCs as they make fast decisions due to strong positive feedback. In this the power consumption and the delay of the conventional, coarse grain and fine grain double – tail comparators are being analyzed and compared with each other.

A. Conventional Double-Tail comparator
B. Coarse grain Double-Tail comparator
C. Fine grain Double-Tail comparator

III. CONVENTIONAL DOUBLE-TAIL COMAPRATOR

The schematic of Conventional Double-Tail comparator is shown in the figure below. In this structure it is having less stacking and because of this it can operate at low supply voltages.

The Double-Tail enables large current in both Mtail2 and latch stage for fast latching independence of the input common mode voltage(Vcm), and for low offset a small current is applied to the input stage.

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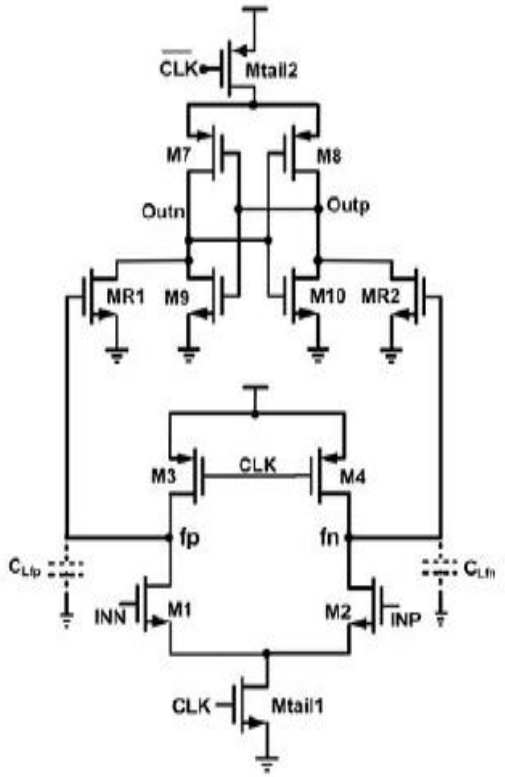
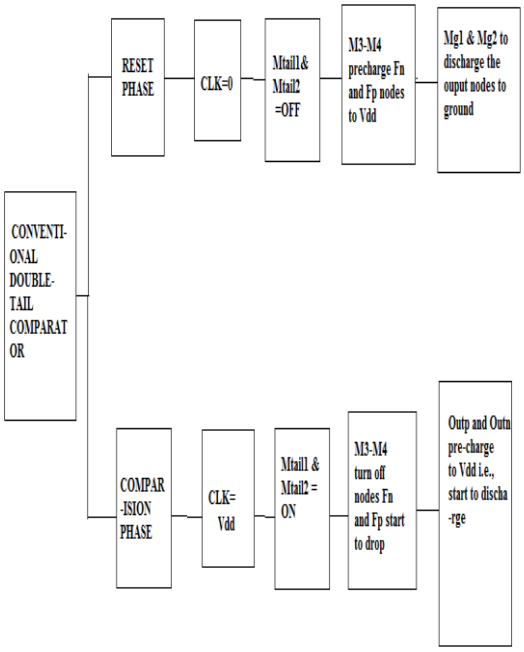


Figure 4: Conventional Double-Tail comparator

Operation:

During the reset stage, that is Clock='0', the Mtail1 and Mtail2 are OFF. The transistors M3,M4 pre-charges to nodes fn and fp to V_{DD} which makes MR_1 and MR_2 to discharge the output nodes Outn and Outp to the ground.

During decision making phase that is Clock='V_{DD}', Mtail1 and Mtail2 are ON and the transistors M3 and M4 turn OFF. The voltage at the nodes fn and fp start to drop with the rate defined by $I_{Mtail\,1/Cfn(p)}$ and an input dependent differential voltage $\Delta Vfn(p)$ will also build up. The intermediate stage formed by the transistor MR_1 and MR_2 passes $\Delta Vfn(p)$ to the cross coupled inverters and provide a good shielding between the output and input to get the reduced kickback noise.



IV. COARSE GRAIN DOUBLE-TAIL COMPARATOR

As long as f_n continuously falling, the corresponding PMOS control transistors mc1 in this case starts to turn on, pulling fp nodes back to the $V_{DD;}$ so another control transistors Mc2 remains off, allowing fn to be discharged completely. In other words unlike conventional double tail dynamic comparators which in Vfn/fp is just functions of input transistors transconductance of input voltage difference in the proposed structures as soon as the comparator detects for the instance nodes fn discharge faster, a PMOS transistors Mc1 turns on, pulling the other nodes fp back to the V_{DD}. Therefore the time passing, the difference between the fn and fp (Vfn/fp) increases in a exponential manner, leading to the reductions of latch regeneration times.

In this evident that the double tail comparator technologies can operates faster and be used in lower supply voltages, while consuming nearly the same powers as the conventional dynamics comparator.

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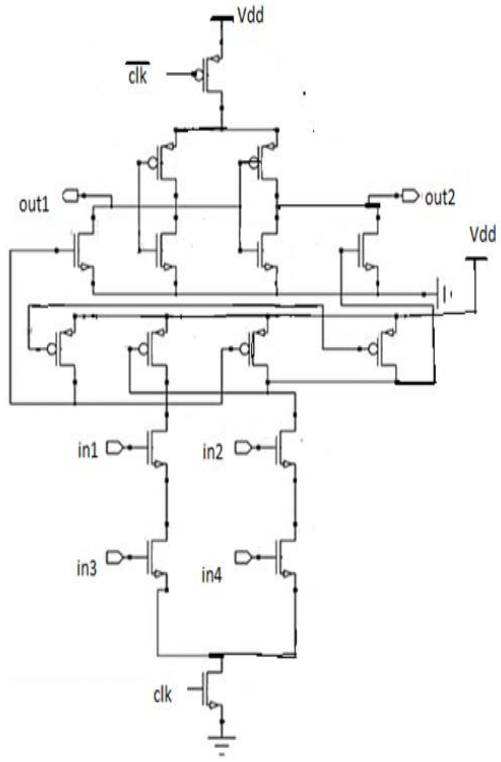

Figure 5: Coarse grain Double-Tail comparator

In this case the power consumption and delay will be reduced when compared to the conventional double-tail comparator.

V. FINE GRAIN DOUBLE-TAIL COMPARATOR

As long as f_n continuously falling, the corresponding PMOS control transistors mc1 in this case starts to turn ON, pulling fp nodes back to the $V_{DD;}$ so another control transistors Mc2 remains OFF, allowing fn to be discharged completely. In other words unlike conventional double tail dynamic comparators which in Vfn/fp is just functions of input transistors transconductance of input voltage difference in the proposed structures as soon as the comparator detects for the instance nodes fn discharge faster, a PMOS transistors Mc1 turns on, pulling the other nodes fp back to the V_{DD}.

Due to the better performance of the double-tail architecture in applications like low voltage, the comparator is designed based on the double-tail structure. The main idea of the comparator is to increase the Vfn/fp to increase the latch regenerative speed. For this purpose, two control transistors Mc1 &Mc2 have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner.

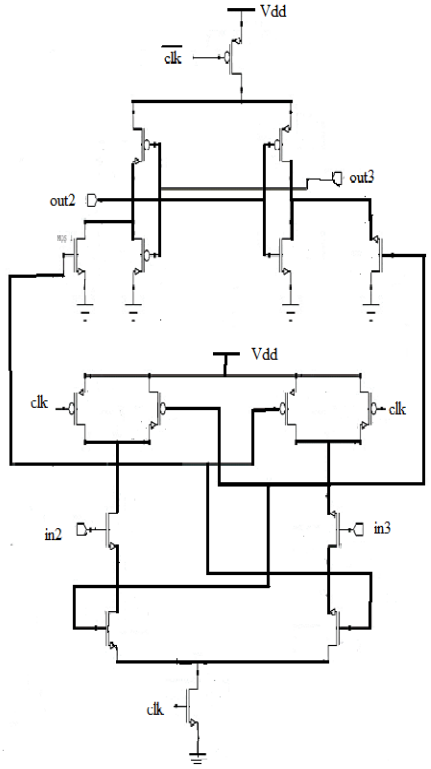

Figure 6: Fine grain Double-Tail comparator

Operation:

During the reset phase, Clock=0 the Mtail1 &Mtail2 are OFF, avoiding static power, M3 and M4 pulls both fn and fp nodes to V_{DD}. Hence transistor Mc1 and Mc2 are cut-off. Intermediatestage transistors MR1 and MR2, reset both the latch outputs Outn and Outp to ground.

During the decision-making phase, the control transistors are still in OFF state. Thus, fn and fp starts to drop with different rates according to the input voltages. Suppose Vinp>Vinn, fn drops faster than fp since M2 provides more currents than M1.

One of the point that should be considered in this circuit is that when one of the control transistors turns ON, a current from V_{DD} is drawn to the ground through input and tail transistor, resulting in static power consumption. To overcome this two NMOS switches are used below the input transistors.

At the beginning of the decision making phase, due to the fact that both fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp node is discharging faster, control transistors will act in a way to increase their voltage difference.

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If the fp is pulling up to the V_{DD} and fn should be discharged completely, hence the switch in the charging path of fp will be opened but the other switch connected to fn will be closed to allow the complete discharge of fn node which means that the operation of the control transistors with the switches emulates the operation of the latch.

VI. SIMULATION

The circuits of the comparators are designed using the Mentor graphics tool with 130nm technology. The schematic diagrams and waveforms of all the comparators are shown below.

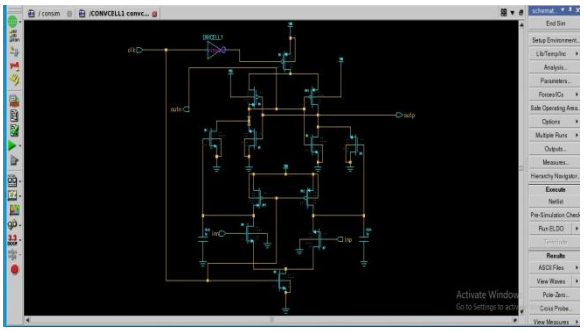

Figure 7(a): Schematic of Conventional Double-Tail comparator

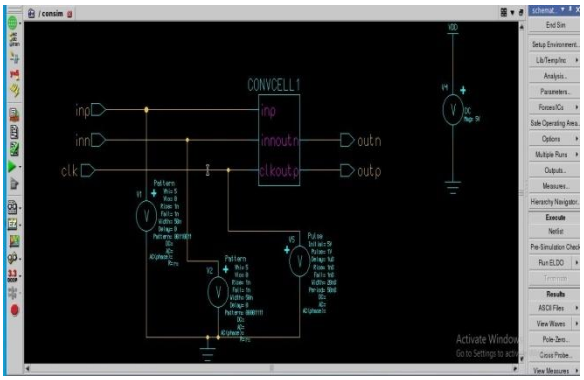

Figure 7(b): Simulation of Conventional Double-Tail comparator

Figure 7(c): Waveforms of Conventional Double-Tail comparator

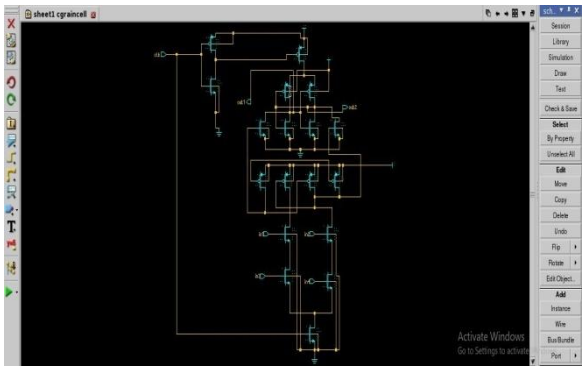

Figure 8(a): Schematic of Coarse grain Double-Tail comparator

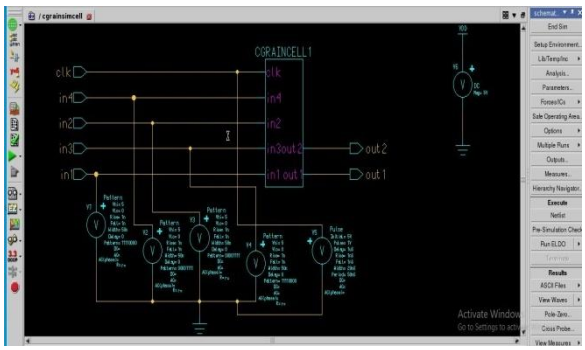

Figure 8(b): Simulation of Coarse grain Double-Tail comparator

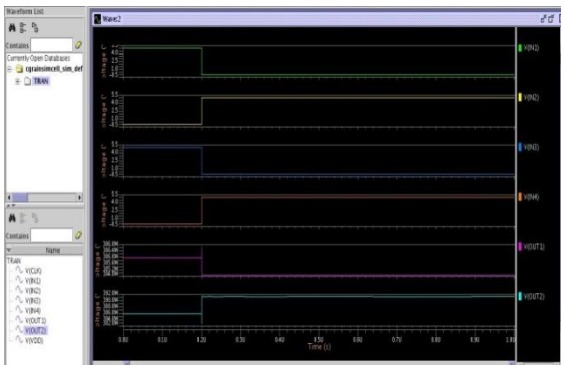

Figure 8(c): Waveforms of Coarse grain Double-Tail comparator

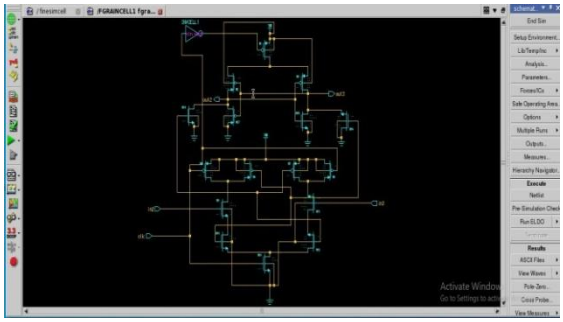

Figure 9(a): Schematic of Fine grain Double-Tail comparator

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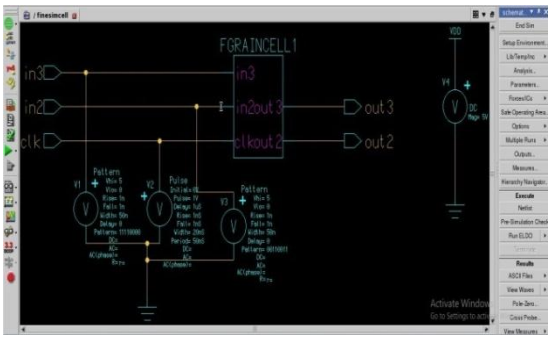

Figure 9(b): Simulation of Fine grain Double-Tail comparator

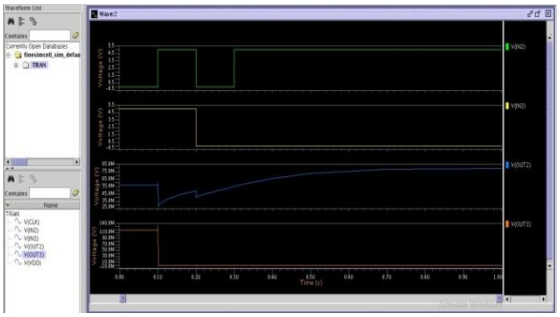

Figure 9(c): Waveforms of Fine grain Double-Tail comparator

VII. PERFORMANCE COMPARISON

The performance comparison given in the below table shows the power dissipation of all the discussed comparators.

TABLE
Performance comparison of various comparators

COMPARATORS	POWER DISSIPATION (NW)
Conventional Double-Tail comparator	136.3870nw
Coarse grain Double-Tail comparator	91.06nw
Fine grain Double-Tail comparator	90.546nw

From the above table, it is observed that the power dissipation of the comparators are reduced significantly.

VIII. CONCLUSION

In this paper, the different double-tail comparators are designed and simulated using Mentor graphics with 130nm CMOS technology. From the result it is observed that the power dissipation and delay is reduced. Hence, these comparators can be used for the design of high speed ADCs as the delay and power are reduced hence resulting in faster operation.

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