International Journal of Advances in Engineering and Management (IJAEM)
Volume 3, Issue 9 Sep 2021, pp: 1251-1254 www.ijaem.net ISSN: 2395-5252

Design Of Low Power Architecture Of Line Coding Schemes

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Submitted: 10-09-2021 Revised: 19-09-2021 Accepted: 23-09-2021

ABSTRACT— Line Coding Schemes are used to tune the waveform in voltage or current levels based on properties of physical channel. Line coding techniques used are Bi-Phase Space Coding (BPSC), Bi-Phase Mark Coding (BMC) and Phase Coding (PC). Our Proposed work is to design the BMC, BPSC, PC generation and degeneration operation circuits. Our second objective is to reduce area and power consumption by modifying the number of MOS devices used by adjusting the width. System is designed in Cadence Virtuoso 180nm technology. Simulation is done in ADE and Layout in Layout Suite XL. our design uses 59 transistors and power can be reduced up to 33% by using any one of the suitable coding schemes among BPSCC, PC and BMC based on type of input data signal. If the input is having 50%duty cycle, PC scheme will be used for power reduction. If high level is more than low level, BPSC scheme is suitable. If low level is more than high level, BMC scheme is suitable.

Keywords—VLSI design, Line coding, BPSC, Low power, BMC, PC.

I. INTRODUCTION

A. BMC or BPSC or PC are used as Line coding techniques for communication system. BMC can be designed by combining BPSC and PC. Our proposed design has architecture of BPSC, BMC and PC schemes in single design. Anyone of the coding schemes can be selected by selecting control input. Users get area and power optimized design. For this, power and area has to be reduced. In present work, area and power had been reduced by changing the number of blocks used to design. Our work decreases number of transistors required to construct each block. As a result, area requirement is reduced by 58.76% and transistors have been reduced by 10.6%.

II. PROPOSED WORK

As mentioned in introduction, design is capable of doing code generation and degeneration operation of BPSC, BMC and PC schemes. Present system has PC and BPSC in a single system. Our work combines BMC with present system and reduces transistor count in schematic. Logic for code degeneration and code generation of BMC scheme has been developed and compared with available system's BPSC schemes logic. The relationship of BMC and BPSC is used to combine BMC with the presently available system without extra hardware requirement.

III. DESIGN OF PROPOSED ARCHITECTURE

Bi-Phase Space Coding is also called FM1 coding. In this coding scheme the encoded data will be of frequency modulation when data input is '1'.and hence FM1 coding.

Architecture Design of BMC Generation

Waveform for BMC generation operation is shown in Fig. 1. Regardless of input bit, there

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will be transition during positive edge of clock. If input bit is '1', there is transition at midpoint of bit in the generated code. If input bit is '0', no transition at the mid of bit. e2 and e1 are values of code when clock cycle is low and high. The four possible levels L1 (01), L0 (00), L3 (11), and L2 (10) present in code.

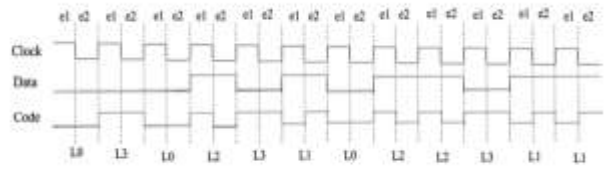

Fig. 1 Bi-Phase Mark Code generation

$$e_1 = \overline{e_2^*}$$

$$e_2 = \bar{D} \cdot \overline{e_2^*} + D \cdot e_2^*$$

$$e_2 = D \odot e_2^*$$

Architecture Design of BMC Degeneration

Waveform for BPMC Degeneration is shown in Fig. 2. If code is changing at half clock or during negative edge of clock cycle, data bit can be predicted as '1'. If code is changing at positive clock, data bit can be predicted as '0'. e2 and e1 are bit value of data during the clock cycle is low and high. There are two levels L1 (11) and L0 (00) in data.

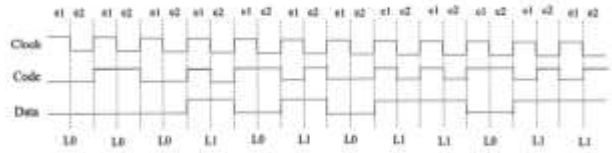

Fig 2: BMC Degeneration architecture

$$D = \overline{e_1} \cdot e_2 + e_1 \cdot \overline{e_2}$$

$$D = e_1 \oplus e_2$$

$$e_1 = \overline{e_2^*}$$

$$e_2 = D \cdot \overline{e_2^*} + \overline{D} \cdot e_2^*$$

Proposed Architecture

Proposed architecture is shown in Fig. 3 where input is given to 'in'. Sel, Cb, Ca, Cd and Cc are used as control inputs. Clock input is given to 'clk' terminal. Generated code is available at X. Degenerated data for BPSC and PC is available at Y. Degenerated data of BMC is available at Z.

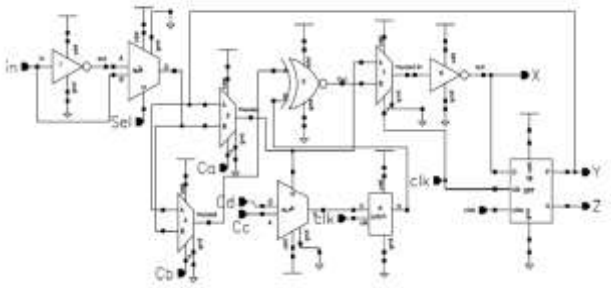

Fig 3: Proposed Architecture Design

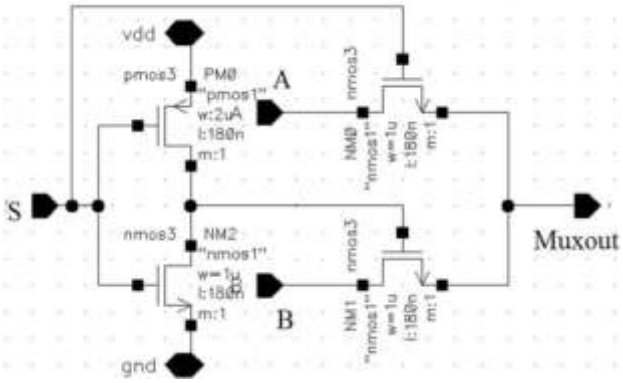

Fig 4: MUX Schematic

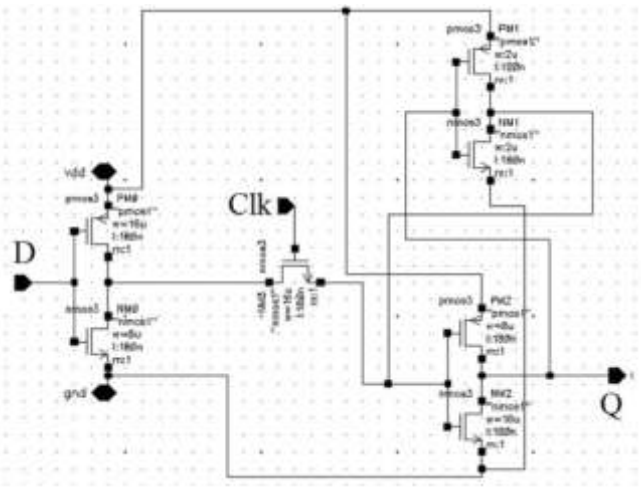

Fig 5: D Latch Schematic

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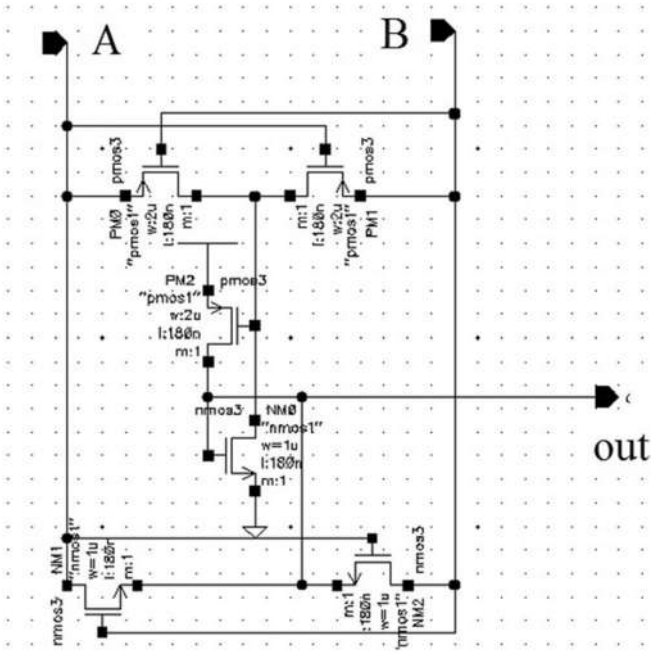

Fig 6: Optimized match finder Schematic

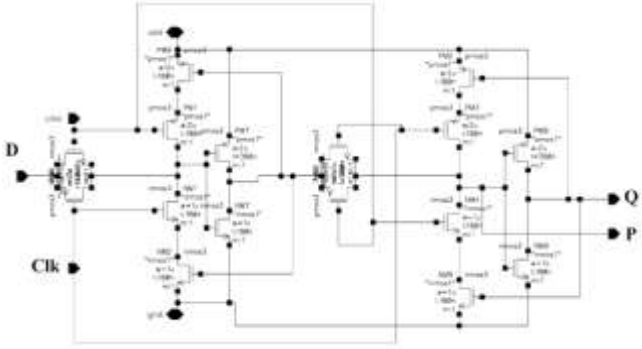

Fig 7: D Flip Flop Schematic

IV RESULT AND DISCUSSION

Power Analysis

Power analysis done at three different frequencies, 100, 250 and 500 MHz. BPSC, BMC design scheme analysis is done in three different cases. PC system is analyzed in a single separate case as the presently available results show BPSC requires more power than PC. Our system shows the BMC consumes less power compared to BPSC. BMC and BPSC consume less power than PC in many different cases. BPSC system is analyzed in three different cases based on input type.

1)BPSC normal case (equal number of high and low signals).

2)BPSC special case 1 (high signal for small duration).

3)BPSC special case 2 (high signal for large duration).

BMC System can be analyzed in three different cases as listed below.

1)BMC normal case (equal number of high and low signals). 2)BMC special case 1 (High signal for small duration).

3) BMC special case 2 (High signal for large duration).

PC system is analyzed in normal case. First of all, BPSC normal case is analyzed. In the normal case, equal number of high and low signals are present in the input. For example, if 10101010101010101010 is applied as input then response will be as shown in fig 8.

Fig 8: BPSC for Normal Case

For BPSC special case 1(high signal for small duration and low signal for large duration in its input). For the input sequence 1000001001000110000 the response is shown in Fig. 9.

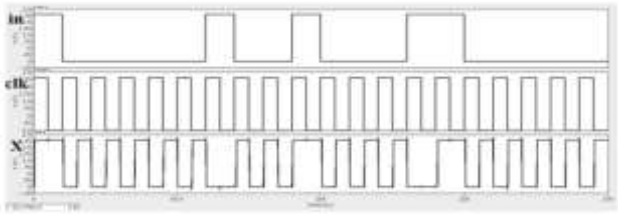

Fig 9: BPSC Special Case 1

BMC Normal case has approximately equal high and low signals. For 10101010101010101010 as input sequence, response is shown in Fig. 10. Where generated code has moderate transition count.

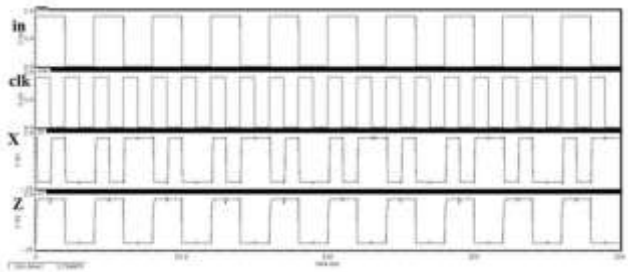

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Fig 10: BMC Normal

BMC special case 1(has high signals of small duration and low signals of large duration). For 00010000001001000110 as input sequence response is shown in Fig. 11.

Fig 11: BMC Special case 1

Response of the PC system for '01010101010101010101' as input is shown in fig 12.

Fig 12: PC system respnse.

V CONCLUSION

Our proposed model deals with design of BMC, BPSC and PC generating and degenerating system. BPSC and PC generation and degeneration is only available in the existing works. A coding system is designed using 59 transistors whereas existing system was designed using 66 transistors. Transistor count is reduced by 10.6%. The schematic was designed in Cadence Virtuoso with 1.8 V as input and simulations were done at 100, 250 and 500 MHz frequency. Power analysis was done for three different cases for different patterns of inputs. If the input data has moderate level of high and low signals, then PC is suitable. If the input is having high signals for less duration, BMC is suitable. If the input is having low signals for more duration, BPSC is suitable.

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