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A review of different techniques used to design a low-noise amplifier

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ABSTRACT-This paper summarizes the review of different methodologies which are employed to design low-noise-amplifier (LNA). As we know that LNA is the most integral part of receivers-front-end block. Some of the useful applications of LNA are Mobile Communication, satellite, WLAN etc. While designing LNA we have to focus on a number of parameters. This review explore some techniques of LNA which are Low-Noise High-Linearity Decoupling Capacitor Technique, Noise Reduction Transformer Technique, Plug and Play Technique, Multimode Input Matching Network Technique, Multi-stage inductive series peaking technique, Self-biased Resistive-Feedback Technique, Inductive Degeneration Technique. These techniques are employed for the reduction of power dissipation in CMOS, better noise performance, high linearity, low insertion loss, high gain and good input/output matching are also obtained by using these topologies.

KEYWORDS- ESD, Low-power, Gain, Low Noise Amplifier (LNA), linearity, Noise Figure (NF), S- parameters, Common-Source (CS).

I. INTRODUCTION

All the circuits are consisted of various electronic-components. The noise is occurred in the circuit due to the alteration in the current and voltages. As we know that LNA is the one of the most integral part of a receiver side because it is used to amplify the signal while minimizing the noise. The noise is created in the circuit by all the successive stages and it is minimized by using LNA. A good LNA is having some properties like extremely high gain, low noise figure, high linearity and maximized compression point. LNA is used in various applications like Satellite communication, mobile communication, WLAN, Wi-Max etc. LNA is used in transceiver for maintaining the SNR as high as possible. While designing LNA we have to deal with several RF parameters and trade-offs between them. Due to the huge advancement in the field of communication, low power RF transceiver attains great demand in various applications like ISM bands(Industrial, Scientific and Medical bands) [1]. As we know that all the mobile devices is working on battery and we need more life time of battery that's why we employ various low-power designing techniques for LNA [2]. Our main goal is to attain maximum consumption of energy lower than few mW. While designing LNA we have to focus on some fundamentals which are Scattering-parameter, DC bias, Linearity, NF, gain, good sensitivity, stability, bandwidth and stability [3].

The paper is organised in following manner: Section II includes the description of different techniques used to design LNA, Section III includes the comparison of various techniques used to design LNA, whereas, the overall conclusion for the reviews is incorporated under Section IV. Now we are going to start from the part of Section II which contains discussion of different techniques used for the maximizing gain and minimizing NF.

II. DESCRIPTION OF DIFFERENT TECHNIQUES

(1) Low-Noise High-Linearity Decoupling Capacitor Technique

The LNA designed using this technique has high gain, low noise and large bandwidth. In this technique gate of P-type MOS is connected to the RF input whereas normally it is connected to the biasing network and a capacitor which is de-coupling it from the rest network, that's why there is no intermodulation of input signal is occurred. Because to this there is declination in the linearity is observed due to the presence of bond-wires. The circuit diagram of LNA using this technique is shown in figure 1 and figure 2. This LNA is designed using 130 nm CMOS technology. The

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power dissipation is 22.1 mW with minimum NF of 1.6 dB and power gain of 12.4 dB [4].

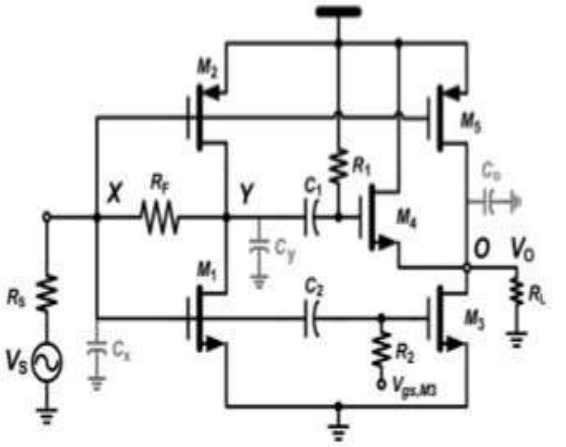

Figure 1: Single-ended circuit diagram of LNA using Low-Noise High-Linearity Decoupling Capacitor Technique [4]

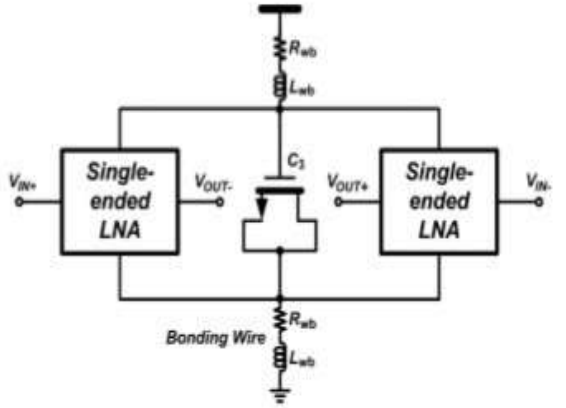

Figure 2: Differential full-circuit of LNA using Low-Noise High-Linearity Decoupling Capacitor Technique [4]

(2) Noise Reduction Transformer Technique

The combination of quadruple-cascode, triple-cascode along with transistor having noise reduction topology was presented. The typical noise reduction transformer topology is shown in figure 3. In this technique for the minimization of noise we employ the noise-reduction transformer along by placing it between the transistor which has a quadruple cascode and triple cascode device, the advantage of this technique is minimization in size, extremely high gain and very low NF. The LNA is designed using 90 nm CMOS process and is operating at Q-band and V-band and it is shown in figure 4. When it is operating at V-band it has a NF of 4.7 dB and maximum gain of 12.7 dB. When it is operating at Q-band it has a NF of 4.6 dB and maximum gain of 20.3 dB [5].

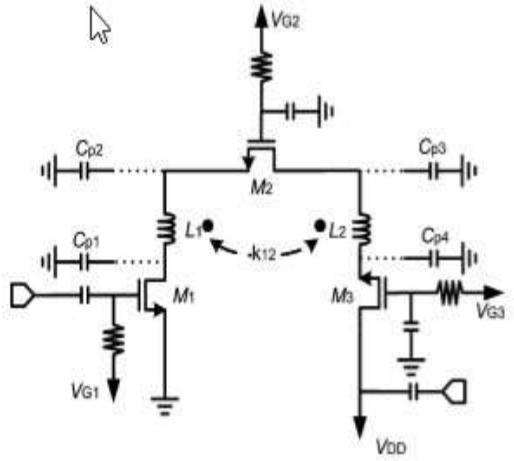

Figure 3: Typical circuit arrangement of noise reduction transformer topology [5]

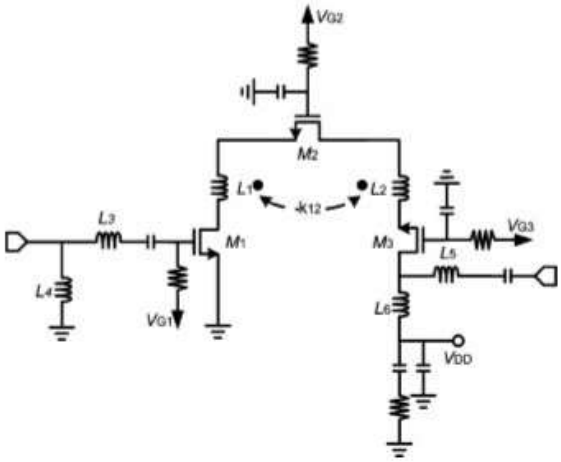

Figure 4: Circuit diagram of LNA using noise reduction transformer topology [5]

(3) Plug and Play Technique

The circuit arrangement of this technique is shown in figure 5. This LNA is designed using 90 nm CMOS technology. This technique is used to avoid the input return loss and insertion loss. For the input/output ESD protection we used an inductor as Plug and Play. The designed LNA has very good noise performance the NF is 2.9 dB, low power dissipation of 9.7mW, high gain and up-to the 1.4 A current it is protected against ESD. That's why the distortion of signal is minimized by using this technique [6].

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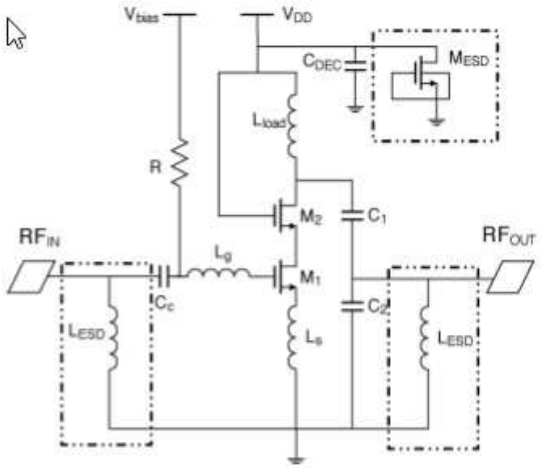

Figure 5: Simplified circuit diagram of LNA using Plug and Play technique [6]

(4)Multi-mode Input Matching Network Technique

The LNA which is designed using this technique is having very high bandwidth. This LNA is having highest BW among the all reported LNAs and has an LNA has ability to work in ultra-wideband, single band and dual band. The LNA designed using this technique is represented in figure6 it has input matching network having multimode that basically formed by the combination of CS configuration with inductive degeneration and switched multi-tap transistor [7].

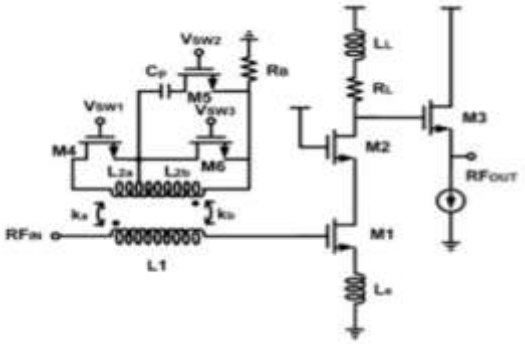

Figure 6: Circuit diagram of LNA using Multimode Input Matching Network Technique [7]

(5)Multi-stage inductive series peaking technique

In this technique feedback path contains a combination of a tuning capacitor in parallel with an inductor to attain ultra wide bandwidth along with good input/output matching. By using this technique we achieve high gain along with excellent gain stability. The resistive feedback topology with triple stage cascaded topology provides a minimal NF of 4.5 dB and maximum gain of 11.5 dB. The propose LNA using this technique is shown in figure 7 [8].

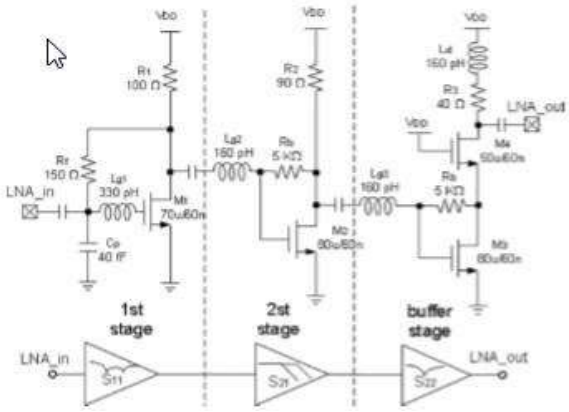

Figure 7: Proposed LNA using multi-stage inductive series peaking [8]

(6)Self-biased Resistive-Feedback Technique

The LNA is designed using 90 nm digital CMOS technology and it has large bandwidth and low power dissipation. Here the modification of this topology is used. For the wideband response the combination of a shunt peaking resistor along with two inductors are connected in feedback path, due to which there is enhancement in the bandwidth. In this technique there is no requirement to use DC block capacitor because in this technique inductive degenerated PMOS is used and in feedback path the inductor is also connected to the feedback path of input transistor. The maximum gain of 12.7 dB with minimal NF of 3.3 dB is obtained by using this technique. The circuit arrangement is shown in figure 8 [9].

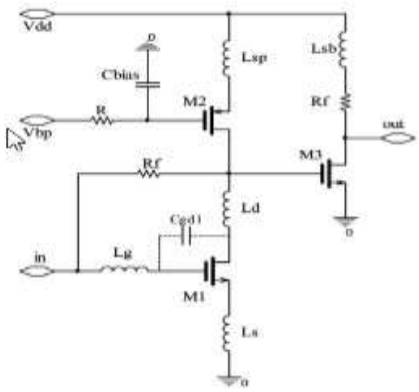

Figure 8: Wideband LNA using self-biased resistive-feedback technique [9]

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(7) Inductive Degeneration Technique

This LNA is designed using 180 nm CMOS technology. This technique is used for improvement of noise performance along with increasing the bandwidth, the power dissipation is also decreased using this technique. The distributed amplifier is cascaded with CS configuration of amplifier to increase the BW and make LNA to operate over wideband. The circuit diagram of LNA using inductive-degeneration technique is shown in figure 9 [10].

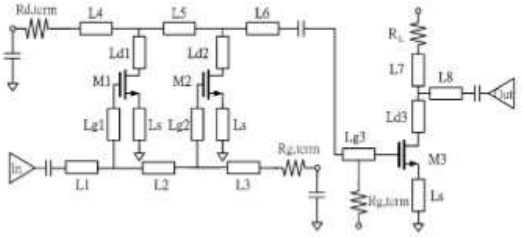

Figure 9: LNA using inductive-degeneration-technique [10]

III. COMPARISON OF DIFFERENT TECHNIQUES USED TO DESIGN LNA

The comparison of different techniques used to design LNA is done on the basis of different LNA parameters and topology used to design that LNA. The comparison is given in Table 1.

Table 1: Comparison of Result

CMOS Process	P_{DC} (mW)	Gain (dB)	F.O.M	NF (dB)	Topology	References
130 nm	22.1	12.4	34.1	1.6	Noise Cancellation circuit and Volterra Series	[4]
90 nm	18	12.7	4.5	4.7	Single-Stage Triple Cascode with Noise Reduction	[5]
90 nm	9.72	13.3	1.36	2.9	Plug and Play Inductor	[6]
130 nm	6.4	14.7-16.4	-	1.9-4.7	Inductively Degenerated Common Source Multitap Transformer	[7]
65 nm	25.5	11.5	29.7	4.5	Cascaded 3-Stage Resistive Feedback	[8]
90 nm Digital CMOS	12.6	12.7	9.43	3.3	Self-Biased Resistive Feedback	[9]
180 nm	7	10	3.13	3.8-6.9	Distributed Amplifier	[10]

IV. CONCLUSION

This Paper is consisted by various techniques of LNA and with its varying NF and gain. We have reported several techniques used for the minimization of noise and maximization of gain. All the reviewed techniques are having their own pros and cons. The selection of topologies is one of the greatest challenge while designing LNA because all the topologies is best applicable for some range of frequency band over which it is operating. While designing LNA we are trying to optimize all the RF parameter simultaneously while dealing with various types of trade-offs. This paper also contains comparison of various LNA designing techniques on the basis of dissipation of power, noise figure, gain and figure of merit. In the future work we are focussing on designing new topologies for decreasing the power dissipation, minimizing noise figure and insertion loss and increasing power gain.

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