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A Review of an ultra-low-power LNA with High power Gain for 5-GHz frequency band applications

Nishant Kumar, Mrs. Rajani Bisht
Electronics and Communication, HBTU, Kanpur, India
Associate Professor, ET Department HBTU, Kanpur India.

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ABSTRACT: In this paper a 180nm CMOS technology is used to design A Low-Power LNA to optimize gain and noise figure at 5-GHz frequency with a supply voltage of 0.63 v. It can be operate at lowest supply voltage with least dc power consumption by using a gain boosting, current-reused and forward-body-bias technique. While combining these techniques we achieve an ultra-low-power LNA.

KEYWORDS: Low noise amplifiers (LNAs), Ultra-low-power, current-reused, forward-body-bias, gain-boosting, noise figure.

I. INTRODUCTION

Radio frequency (RF) industry grows substantially more after the Darwinism in communication. Radio frequency technologies sought out later the Facilitate of RC by Guglielmo Marconi and Tesla. Preliminary to Darwinism in wireless communication RF technology was extremely considerate in industry of defence. The appealing linkage of industry of electronic device and communication makes microwave radio frequency engineering extremely incentive and productive.

Now speed of Wi-Fi standards on 5-GHz bands is more than other frequencies like as on 2.4-GHz, and this paper is also designed at 5-GHz frequency. There are many CMOS LNA circuits are demonstrated in last few years [1]-[10].

For minimizing the power dissipation (Pdc), some of the techniques are used name as follows:

Transformer-coupled feedback Gain boosting [5], Current reused [1] and forward-body-bias [2].

The rest of this paper is organized as follows: Designing and implementing of Linearly ultra-low-power LNA in Section II, Results in Section III and finally conclusion are presented in Section IV.

II. CIRCUIT DESCRIPTION

The schematic of an ultra-low-power LNA with applying all the three techniques is shown in circuit diagram figure 1 and the circuit parameters are in table 1. From its equivalent small-signal model, noise and transconductance is measured as

$$\boldsymbol{F = 1 + \frac{\gamma}{\alpha}\frac{1}{(1+A)}} \qquad \textbf{(1)}$$

$$\boldsymbol{G_m = (1 + nk)g_m} \qquad \textbf{(2)}$$

If we have to find gain-boosting component, A=nk, then it can be find out by the coupling component and turns ratio of the transformer. The functional transconductance rises by (1+A) times due to transformer coupling and by the same factor (1+A) it decreases the noise figure and through source to gate –A is denoted as gain.

To operate the LNA at low supply voltage and low power dissipation with sufficient gain we add a technique in the gain boosted common-gate stage named as forward-body-bias.

The threshold voltage of MOSFET is as follows [6]:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\varphi_f - V_{bs}} - \sqrt{2\varphi_f}\right) \qquad (3)$$

For low dc power consumption with high power gain we combine all three techniques transformer-coupled feedback gain boosting, current reused and forward body bias techniques.

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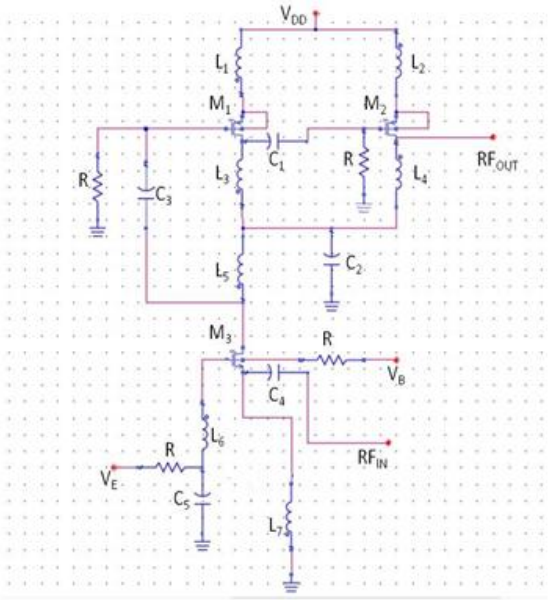

Fig.1 Schematic of proposed ultra low power LNA

TABLE I: Parameters of proposed LNA

Devices	Values
M_1 / M_2	64 µm / 0.18µm
M_3	46 µm / 0.18µm
R	10 K
L_1 / L_2	0.2 nH
L_3 / L_4	3.7 nH / 3.5 nH
L_5	3.4 nH
L_7 / L_6	6.4 nH/5.4 nH
C_1/ C_3	2 pF
C_2	20 pF
C_4	4 pF
C_5	8 pF

III. SIMULATION RESULTS

This ultra low power LNA is based on 5-GHz band applications. This LNA has been designed and simulated in CMOS 180 nm process. In this LNA drain voltage are 0.63 V and gate-bias voltages are 0.5 V and body-bias voltages of LNA is 0.3 V. current consumption of this circuit is 772µA at supply voltage 0.63 V. In this LNA the power dissipation (Pdc) is 0.486 mW and simulated results are shown in Fig.2, 3, 4.

As we see S- parameters in fig 2 and 3 we can see gain of this LNA is 16.47 dB and input return loss (S_{11}) is

-9.01 dB and noise figure (NF) in fig 4 is 3.5 dB.

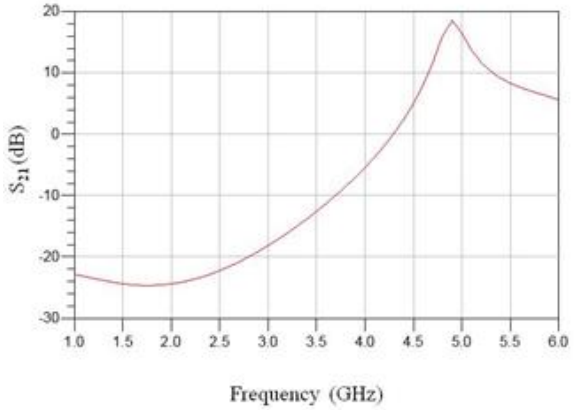

Fig.2 S_{21}: 16.47 dB

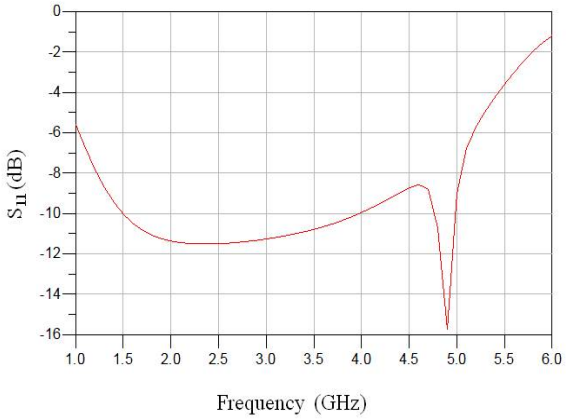

Fig.3 S_{11}: -9.01 dB

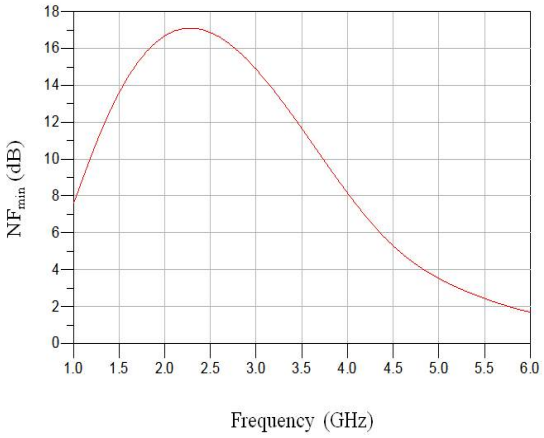

Fig.4 NF: 3.5 dB

In this LNA the output of 1-dB compression point (P1 dB) is -18.7 dBm and and 3dB bandwidth is 0.7 GHz.

TABLE II: COMPARISON TABLE OF PREVIOUSLY REPORTEDN CMOS LNAs

References	[5]	[6]	[7]	This work
Process (nm) CMOS	180	180	180	180
Supply Voltage (V)	0.63	0.6	1.2	0.63
Pdc (mW)	0.387	0.336	1.66	0.486
BW (GHz)	0.5	0.45	0.5	0.7
Frequency(GHz)	5.0	4.8	3.5	5.0
Gain (dB)	14.7	10	12.5	16.47
NF (dB)	4.3	4.8	3.6	3.5

IV. CONCLUSION

In this paper a 5-GHz ultra-low power LNA is presented by using 0.18µm CMOS process. In the starting by using all the techniques gain boosting, current-reused and forward-body-bias this ultra-low power LNA at 5-GHz frequency gives NF and power gain of 4.3 dB and 14.7 dB simultaneously. but after then we optimized this circuit by using all the three techniques as discussed above and then this LNA gives best result as gain of 16.47 dB and NF of 3.5 dB with low supply voltage of 0.63 V and the dc power consumption is 0.486 mW.

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