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8-Bit Arithmetic Logic Unit Design using Modified Gate Diffusion Input (m-GDI) Technique

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ABSTRACT— In this paper, the map of an 8-bit Arithmetic Logic Unit (ALU) using modified Gate Diffusion Input (MGDI) technique is presented. Implementing the GDI technique in designing the arithmetic logic unit results in ultra low power consumption and the number of gates it requires is much less. Which result in reduced power consumption and reduced chip-area, most important object in digital VLSI design. In this design, 3 transister XOR is used in the FA(full adder). Moreover, a novel 1-to-8 de-MUX circuit has been used in the design. Few number of research papers are studied and compared with logic families and then finally come up with an 8-bit ALU which can perform 8 type of operations.

I. INTRODUCTION

The main part of a computer is Central Processing Unit (CPU). In that the main part is the Arithmetic Logic Unit (ALU) [1] which performs all kinds of operation like addition, subtraction, multiplication, division and logical operations such as Inversion, OR, AND, XOR, Multiplexing and may other operation. Any device capable of processing needs an arithmetic logic unit (ALU) be it a application specific smaller circuits or VLSI chip. Improving the design of the arithmetic logic unit results in substantial improvement in overall performance and power requirements.

Low power dissipation and compact implementation and are the basic objectives in digital design and complicated circuits, arithmetic logic units are no exception. A effort has been given over the past 20 decades to make conventional CMOS based circuits more power-efficient [2-4] and compact. Subsequently, pass Transistor Logic, domino Logic, Transmission Gate Logic, double Pass Transistor Logic, and many other techniques have been implemented and developed to improve the performance of CMOS based circuits [5-7].

Gate Diffusion Input (GDI) technique is a new design for designing circuits which reduces the power requirement[8]. Also, gate diffusion input (GDI) results in a required number of transistors, which makes for a decrease in chip-size.

There are only 2 transistors in a basic gate diffusion input (GDI) cell - an NMOS and a PMOS. It has four terminals- P, G, N and D; the first 3 act as input terminals [9]. But, a issue with GDI technique is that it has full swing problem [10**]**. It happens because the P-MOS Produces a weak logic 0 and

N-MOS produces a weak logic 1. This problem is overcome by modifications to the existing gate diffusion input GDI technique. The M-GDI technique turns out to be more efficient.

Also, using the M-GDI technique an XNOR gate can be made using 3 transistors only [12-14]. The various conventional designs of the XNOR gate use more than 3 transistors, as can be seen in [16]. The number of transistors required to design CMOS full adder (FA) is 28 [18]. With the help of the 3 transistor XNOR a full adder (FA) can be designed using only 8 transistors [12].

In this paper uses a novel 1-to-8 de-MUX design leveraging the GDI technique, to activate the selection of only the desired module in the arithmetic logical unit ALU.

The most important segments of the m-GDI ALU are:-

- **Arithmetic Unit (AU): -** In this unit performs basic arithmetic operations(AO)- like, subtraction and addition.
- **Logical Unit (LU): -** In this unit carries out logical operations. So the logical operations are AND, OR, NOT, NAND, NOR gates.

II. M-GDI AND GDI

The basic primitive cell in GDI and in M-GDI are similar to the CMOS implementation of

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the inverter (INV) circuit [13]. But, it is able of doing much more than CMOS. It depending on the inputs given to N, G and P the functionality of the circuit varies. G is the common for the N-MOS and P-MOS. N is the source(S) terminal of the N-MOS and P is the source(S) terminal of the P-MOS. All of them acts as input(IN) terminals. The output is obtained from the common drain D [9**]**. The design of a basic GDI primitive cell is shown in Fig. 1.

The basic primitive GDI cell itself can perform a main of functions. The outputs and the inputs have been presented in a table format in TABLE-I. We can say that in spite of being capable of single handedly carrying out such a many number of logical operations the GDI cell has a very few problems.

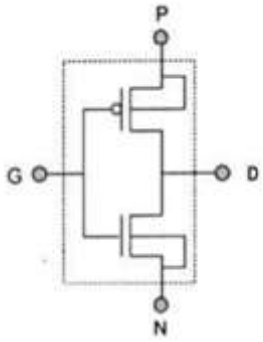

Fig. 1: A Basic GDI primitive cell

TABLE I: FUCTIONALITIES OF THE PRIMITIVE CELL

P	**N**	**G**	**Output**	**Function**
1	0	A	A’	NOT
0	B	A	AB	AND
B	1	A	A+B	OR
B	0	A	A’B	Function 1
1	B	A	A’+B	Function 2
A	B	S	AS+ BS’	2:1 MUX
A	B’	B	A’B+ AB’	XOR
A	B	B’	AB+ A’B’	XNOR

The problem is the most difficulty in fabrication of IC using existing C-MOS technologies [15]. As said earlier there is the problem of full-swing degradation.

To over look these problems, a modified (M-GDI) version of the GDI cell has been designed.

In the M-GDI cell the balk terminals of the N-MOS and the P-MOS are connected to GND and source (VDD) respectively

In the arithmetic logical unit (ALU) developed some of the logical operation have been designed using the m-GDI and others using GDI. The circuit design of a basic cell primitive m-GDI has been shown in Fig-2.

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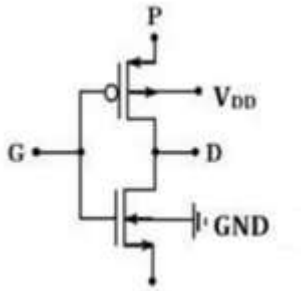

Fig. 2: A Basic m-GDI primitive cell.

III. 3T XOR

Using M-GDI the XOR gate can be designed employing only 3 transistors (3T) as shown in [12-14], in GDI it will take only 2 transistors (2T). The 3 transistors (3T) XOR design is shown below in Fig-3.

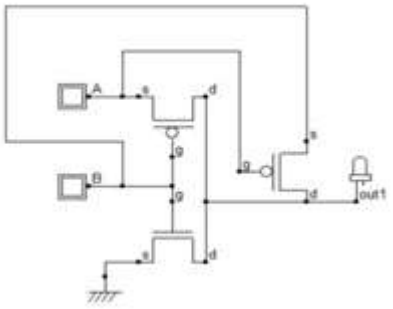

Fig. 3: The 3T XOR design using m-GDI

Every XOR gates which is used in the proposed ALU are 3 transistors (3T) XOR gates. This has resulted in a substantial reduced total power consumption and in the number of total transistors (T) in the entire diagram.

The other input (B) is fed to the common gate input terminal of both the P-MOS and the N-MOS as well as to the source terminal of the P-MOS other one input (A) is fed to both the source and the gate terminals of P-MOS in order to implement the XOR. The common drain (D) terminal of the transistors (T) acts as the output terminal.

The obtained 3-T XOR has a very small delay of 1 transistor (T) only. But, it comes with the full swing problem that the output logic level may sometimes get skewed. However, Dan Wang et al has explained in [14] that by varying the W/L ratio the desired logic level at output can be obtained at all times.

The full adder (FA) [12] and full subtractor (FS) [13] designed using this 3-T XOR are shown below in Fig-4 and Fig-5 respectively.

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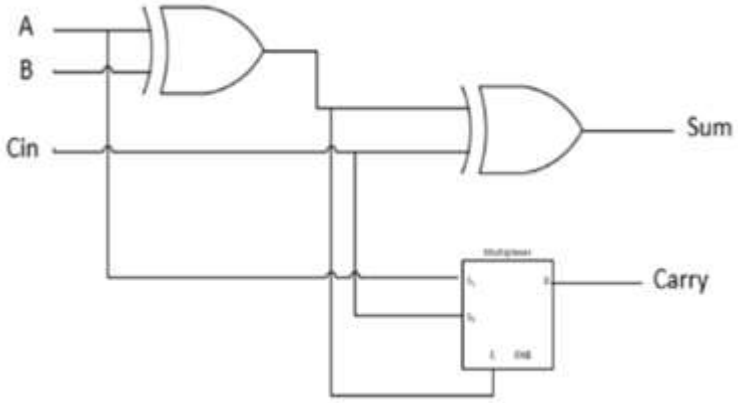

Fig. 4: 8T Full Adder

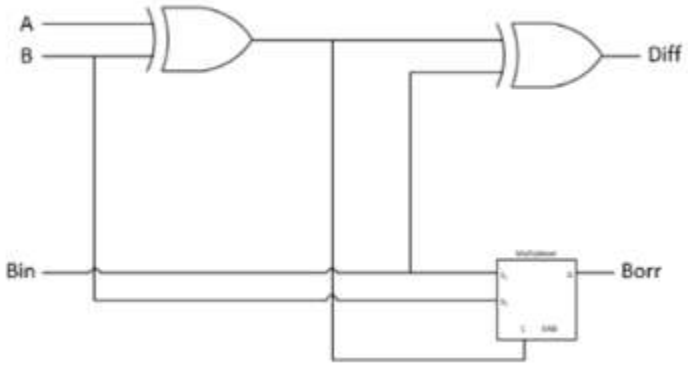

Fig. 5: 8T Full Subtractor

IV. COMPONENTS OF THE PROPOSED ALU

OR, AND, NOT & NAND gates, Comarator, MUX, buffer design have been shown using GDI [8,13,17]. Diagrams of these circuits are shown below from Fig. 6 to Fig. 11:

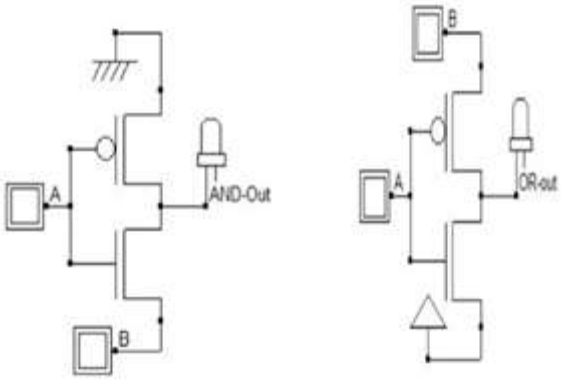

Fig. 6 : 2T AND & 2T OR using GDI

Portion of the desired input when required is facilitated by implementing a buffer (BUF) circuit. The BUF circuit secures the full-swing of output as well as adds a little parasitic delay which adds the more gate delay to other logic circuit while working with other large circuits. The buffer circuit has been shown in Fig-11.

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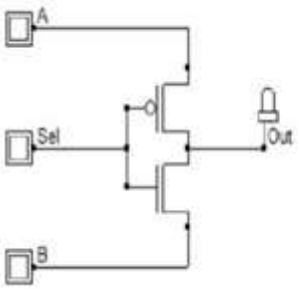

Fig. 7: 2T MUX using GDI

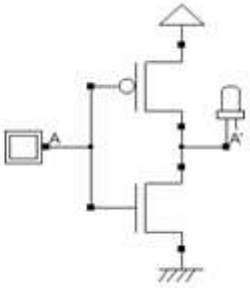

Fig. 8: 2T NOT using GDI

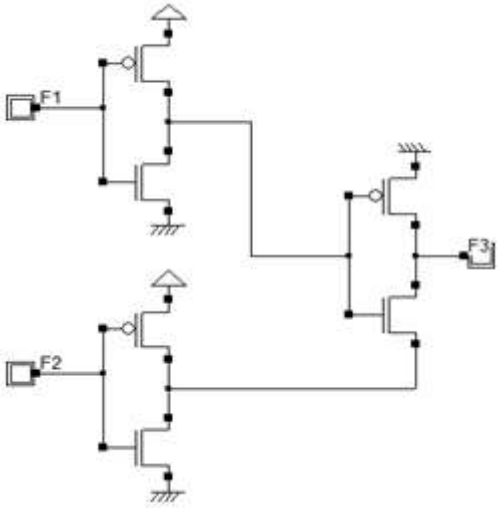

Fig. 9: Comparator using GDI

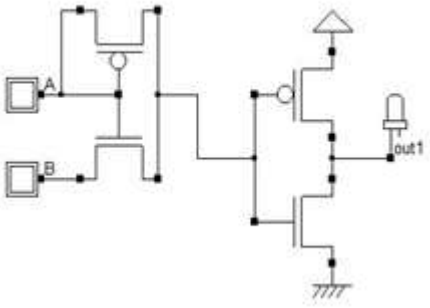

Fig. 10: NAND using GDI

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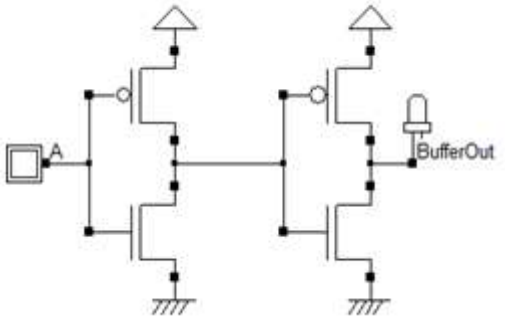

Fig. 11: Buffer Circuit

So far, all the basic cell blocks of the arithmetic logic unit (ALU) have been explained, now it is most important to obtain a logic design that would allow us to choose any one from all the arithmetic unit(AU) and logical unit (LU). For this, taken a 1-to-8 de-MUX which will work in tandem with sixteen sleep transistors (2 for each module) to choose and enable the desired circuitry.

The de-MUX design is a novel design, in that which has been designed using GDI cells. The circuit diagram is shown below.

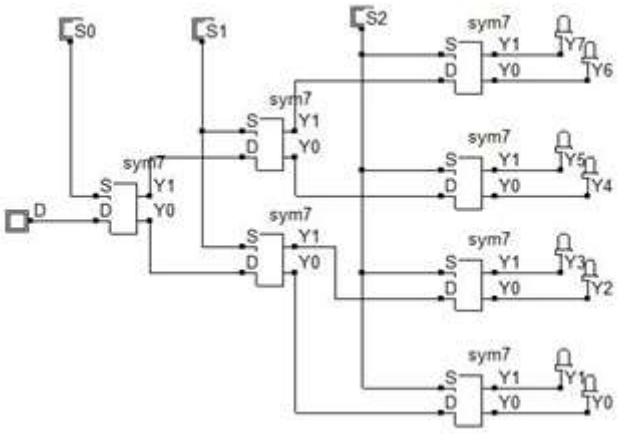

Fig. 12: 1-to-8 Demultiplexer using GDI

The internal circuit diagram (CD) of the identical blocks used 14 times is given below. It is nothing but a simple 1-to-2 de-MUX implemented using gate diffusion input (GDI).

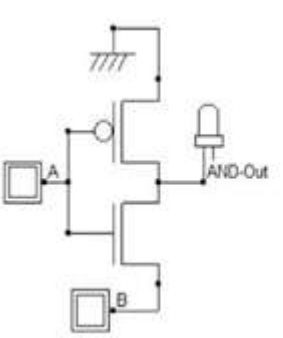

Fig. 13: 1:2 DEMUX using GDI

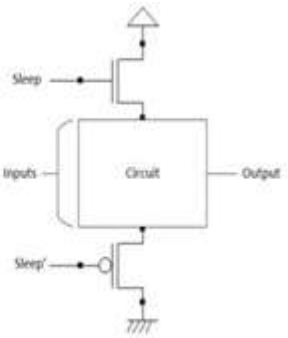

Fig. 14: Sleep Transistor

Clocked type sleep transistors (T) are used to keep design in standby mode. In normal standby mode condition when the signal Sleep=0 or clock=0 the sleep transistors are turns on and they

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allow the logic to evaluate. However, in the paper for our convenience have reversed it, that is in this design the sleep or clock transistors will be on when Sleep=1 or clock=1. The block diagram of sleep transistors is shown above.

Combing up all these logic unit (LU) and arithmetic unit (AU) together got the complete arithmetic logic unit (ALU) block diagram as shown in Fig-15. For the convenience in explaining, internal component of vital modules has been replaced with block diagrams. However, we have detailed circuit diagrams of all the blocks have been given.

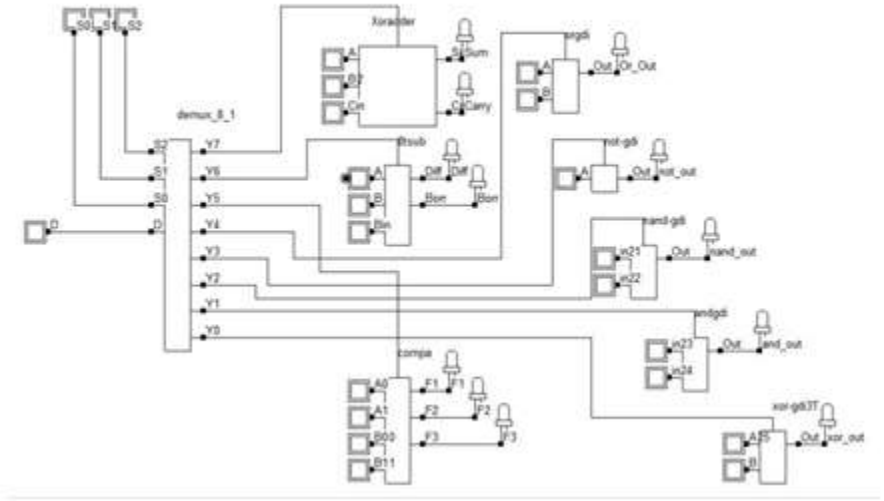

Fig. 15: The complete proposed ALU circuit

V. RESULT & SIMULATION

The simulations have been obtained using Xilinx ISE, starting from transistor level design and further verified using Xilinx ISE 14.7 environment.

The simulation results and with their operation of all the individual gates are realized using m-GDI, GDI and CMOS logic have been explained.

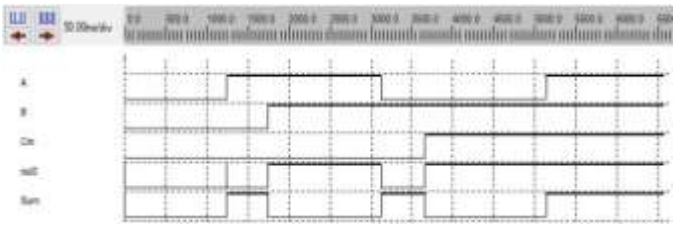

Fig. 16: 8T Full Adder Simulation Waveform

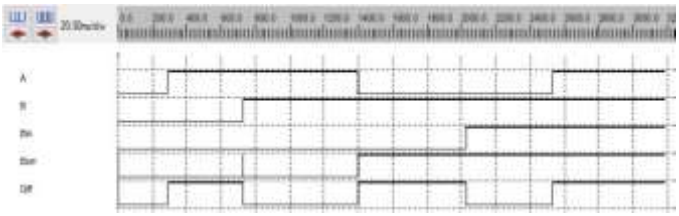

Fig. 17: 8T Subtractor Simulation Waveform

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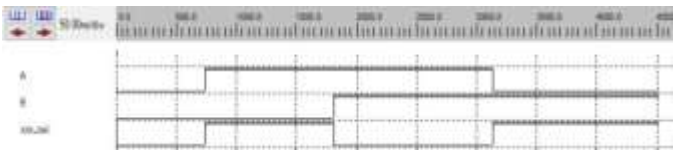

Fig. 18: 3T XOR Simulation Waveform

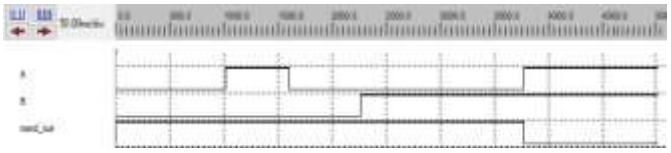

Fig. 19: NAND Simulation Waveform

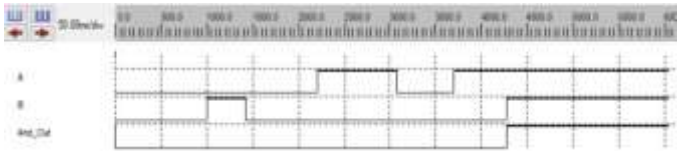

Fig. 20: AND Simulation Waveform

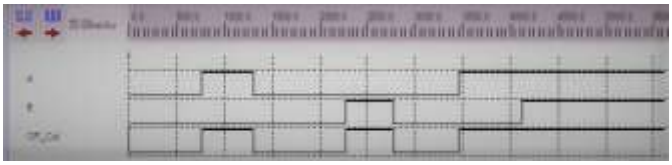

Fig. 21: OR Simulation Waveform

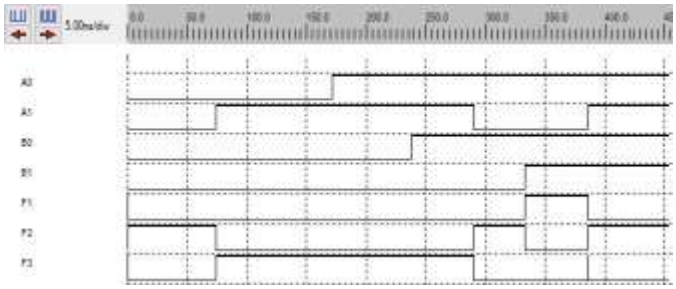

Fig. 22: Comparator Simulation Waveform

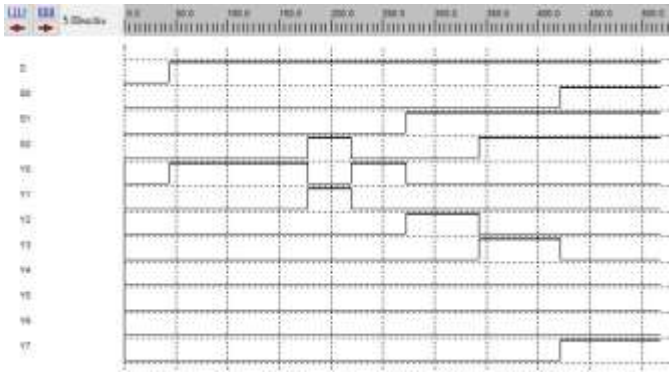

Fig. 23: 1-to-8 Demultiplexer Simulation Waveform

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The simulation of the final ALU circuit as seen in Xilinx ISE 14.7 is shown below.

Fig. 24: ALU Simulation – I

Fig. 25: ALU Simulation – II

Fig. 26: ALU Simulation – II

VI. CONCLUSION

Table II shows a analysis of our proposed circuit with the other two models into consideration which have been discussed in [8] and [11].

TABLE II: COMPARITIVE ANALYSIS OF ALUS

Type of ALU (Design)	**Power (uW)**	**Delay (Critical Path) – (ns)**	**Number of Transistors Required**
8-Bit ALU [8]	38.9	6.95	804
8-Bit ALU [11]	43.8	6.01	785
Proposed Model	31.57	4.57	760

The table shows that the proposed arithmetic logic unit (ALU) not only has the very least number of transistors (T), but also, outperforms the rest in terms of critical path delay and power. Thus it is observed that the proposed model is very efficient compared to the CMOS logical.

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